# Table of Contents

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preface</td>
<td></td>
<td>vii</td>
</tr>
<tr>
<td>Acknowledgement</td>
<td></td>
<td>viii</td>
</tr>
<tr>
<td>Workshop Organizing Committee</td>
<td></td>
<td>ix</td>
</tr>
<tr>
<td>Program Committee</td>
<td></td>
<td>x</td>
</tr>
</tbody>
</table>

## Section 1: Test

- Software-Based On-Line Test of Communication Peripherals in Processor-Based Systems for Automotive Applications  
  P. Bernardi, L. Bolzani, A. Manzone, M. Osella, M. Violante, and M. Sonza Reorda  
  Page 3

- Circuit Profiling Mechanisms for High-Level ATPG  
  Jorge Campos and Hussain Al-Asaad  
  Page 9

- Functional Test Selection for High Volume Manufacturing  
  Vijay Gangaram, Deepa Bhan, and James K. Caldwell  
  Page 15

- Test Calculation for Logic and Delay Faults in Digital Circuits  
  József Sziray  
  Page 20

## Section 2: Verification and Test Generation

- Directed Micro-architectural Test Generation for an Industrial Processor: A Case Study  
  Heon-Mo Koo, Prabhat Mishra, Jayanta Bhadra, and Magdy Abadir  
  Page 33

- Advanced SAT-Techniques for Bounded Model Checking of Blackbox Designs  
  Marc Herbstritt, Bernd Becker, and Christoph Scholl  
  Page 37

- Embedded Software Validation: Applying Formal Techniques for Coverage and Test Generation  
  Tamarah Arons, Elad Elster, Terry Murphy, and Eli Singerman  
  Page 45

- Challenges in System on Chip Verification  
  Noah Bamford, Rekha K Bangalore, Eric Chapman, Hector Chavez, Rajeev Dasari, Yinfang Lin, and Edgar Jimenez  
  Page 52

## Section 3: Architectural and Design Issues

- Workload Slicing for Characterizing New Features in High Performance Microprocessors  
  Hassan Al-Sukhni, David Lindberg, James Holt, and Michele Reese  
  Page 61

- Deep vs. Shallow, Kernel vs. Language – What is Better for Heterogeneous Modeling in SystemC?  
  Hiren D. Patel and Sandeep K. Shukla  
  Page 68

- Statistical Static Timing Analysis Considering the Impact of Power Supply Noise in VLSI Circuits  
  Hyun Sung Kim and D. M. H. Walker  
  Page 76
SECTION 4: DESIGN ERROR DEBUG & DIAGNOSIS

Debug Support for Scalable System-on-Chip ........................................................................................................ 83
  Jianmin Zhang, Ming Yan, and Sikun Li

Abstraction and Refinement Techniques in Automated Design Debugging .......................................................... 88
  Sean Safarpour and Andreas Veneris

Diagnosing Silicon Failures Based on Functional Test Patterns .................................................................................. 94
  Chia-Chih Yen, Ten Lin, Hermes Lin, Kai Yang, Tayung Liu, and Yu-Chin Hsu

AUTHOR INDEX ...................................................................................................................................................... 99