



**INTERNATIONAL  
TEST CONFERENCE  
2008**

**PROCEEDINGS**



**October 28 – October 30, 2008  
Santa Clara Convention Center  
Santa Clara, California USA**



Sponsored by IEEE Computer Society  
Test Technology Technical Council  
and  
IEEE Philadelphia Section



# TABLE OF CONTENTS

## **SESSION 1 DEALING WITH OUTLIERS AND VARIATION IN TODAY'S ICS**

<b>A Study of Outlier Analysis Techniques for Delay Testing</b> .....	1
<i>S. H. Wu, D. Drmanac, L. C. Wang</i>	
<b>Production Multivariate Outlier Detection Using Principal Components</b> .....	11
<i>P. M. O'Neill</i>	
<b>Unraveling Variability for Process/Product Improvement</b> .....	21
<i>A. Gattiker</i>	

## **SESSION 2 MICROPROCESSOR TEST**

<b>The Test Features of the Quad-Core AMD Opteron Microprocessor</b> .....	30
<i>T. Wood, G. Giles, C. Kiszely, M. Schuessler</i>	
<b>DFX of a 3rd Generation, 16-core/32-thread UltraSPARC CMT Microprocessor</b> .....	40
<i>I. Parulkar, S. Anandakumar, G. Agarwal, G. Liu, K. Rajan, F. Chiu, R. Pendurkar</i>	
<b>Test Access Mechanism for Multiple Identical Cores</b> .....	50
<i>G. Giles, J. Wang, A. Sehgal, K. J. Balakrishnan, J. Wingfield</i>	

## **SESSION 3 EMBEDDED MEMORY DIAGNOSIS AND CHARACTERIZATION**

<b>High Throughput Diagnosis via Compression of Failure Data in Embedded Memory BIST</b> .....	60
<i>N. Mukherjee, A. Pogiel, J. Rajski, Jerzy Tyszer</i>	
<b>A History-Based Diagnosis Technique for Static and Dynamic Faults in SRAMs</b> .....	70
<i>A. Ney, A. Bosio, L. Dillillo, P. Girard, S. Pravossoudovitch, A. Virazel, M. Bastian</i>	
<b>Analysis of Retention Time Distribution of Embedded DRAM – A New Method to Characterize Across-Chip Threshold Voltage Variation</b> .....	80
<i>W. Kong, P. C. Parries, G. Wang, S. S. Iyer</i>	

## **SESSION 4 HIGH-SPEED I/O TESTING IN THE REAL WORLD**

<b>External Loopback Testing Experiences with High Speed Serial Interfaces</b> .....	87
<i>A. Meixner, A. Kakizawa, B. Provost, S. Bedwani</i>	
<b>Low cost testing of multi-GBit device pins with ATE assisted loopback instrument</b> .....	97
<i>W. A. Fritzsche, A. E. Haque</i>	
<b>Efficient High-Speed Interface Verification and Fault Analysis</b> .....	105
<i>T. Nirmaier, J. T. Zaguirre, E. L. C. Hong</i>	

## **SESSION 5 DEFECT AVOIDANCE AND COST MODELING**

<b>Implementation Update: Logic Mapping On SPARC Microprocessors .....</b>	<b>114</b>
<i>A. Vij, R. Ratliff</i>	
<b>Failing Frequency Signature Analysis.....</b>	<b>124</b>
<i>J. Lee, E. J. McCluskey</i>	
<b>A Cost Analysis Framework for Multi-core Systems with Spares.....</b>	<b>132</b>
<i>S. Shamshiri, P. Lisherness, S. J. Pan, K. T. Cheng</i>	

## **SESSION 6 DELAY TESTING AND CHIP PERFORMANCE MAXIMIZATION**

<b>Scan Based Testing of Dual/Multi Core Processors for Small Delay Defects .....</b>	<b>140</b>
<i>A. D. Singh</i>	
<b>On-chip Programmable Capture for Accurate Path Delay Test and Characterization .....</b>	<b>148</b>
<i>R. Tayade, J. A. Abraham</i>	
<b>An Automatic Post Silicon Clock Tuning System for Improving System Performance based on Tester Measurements.....</b>	<b>158</b>
<i>K. Nagaraj, S. Kundu</i>	

## **SESSION 7 ATPG AND SAT**

<b>CONCAT: CONflict Driven Learning in ATPG for Industrial designs.....</b>	<b>166</b>
<i>S. Bommu, K. Chandrasekar, R. Kundu, S. Sengupta</i>	
<b>SAT-based State Justification with Adaptive Mining of Invariants .....</b>	<b>176</b>
<i>W. Wu, M. S. Hsiao</i>	
<b>RTL Error Diagnosis Using a Word-Level SAT-Solver .....</b>	<b>186</b>
<i>S. Mirzaeian, F. Zheng, K. T. T. Cheng</i>	

## **SESSION 8 HIGH-PERFORMANCE INTERFACING**

<b>Embedded Power Delivery Decoupling in Small Form Factor Test Sockets .....</b>	<b>194</b>
<i>O. Vikinski, S. Lupo, G. Sizikov, C. Y. Chung</i>	
<b>Measurement Repeatability for RF Test Within the Load-board Constraints of High Density and Fine Pitch SOC Applications.....</b>	<b>202</b>
<i>T. P. Warwick, G. Rivera, D. Waite, J. Russell, J. Smith</i>	
<b>Wafer-Level Characterization of Probecards using NAC Probing .....</b>	<b>212</b>
<i>G. Y. Kim, E. Byunb, K. Kangb, Y. Junc, B. Kong</i>	

## **SESSION 9 POWER-AWARE DFT METHODS**

<b>A Power-Aware Test Methodology for Multi-Supply Multi-Voltage Designs .....</b>	<b>221</b>
<i>V. Chickermane, P. Gallagher, J. Sage, P. Yuan, K. Chakravadhanula</i>	
<b>Peak Power Reduction Through Dynamic Partitioning of Scan Chains.....</b>	<b>231</b>
<i>S. Almukhaizim, O. Sinanoglu</i>	

<b>Power-Aware At-Speed Scan Test Methodology for Circuits with Synchronous Clocks</b> .....	241
<i>B. Nadeau-Dostie, K. Takeshita, J. Côté</i>	

## **SESSION 10 OPENS + SHORTS**

<b>Time-dependent Behaviour of Full Open Defects in Interconnect Lines</b> .....	251
<i>R. Rodríguez-Montañés, D. Arumí, J. Figueras, S. Eichenberger, C. Hora, B. Kruseman</i>	
<b>Statistical Yield Modeling for Sub-wavelength Lithography</b> .....	261
<i>A. Sreedhar, S. Kundu</i>	
<b>Detection of Internal Stuck-open Faults in Scan Chains</b> .....	269
<i>F. Yang, S. Chakravarty, N. Devta-Prasanna, S.M. Reddy, I. Pomeranz</i>	

## **SESSION 11 ADVANCES IN BOARD INTERCONNECT TEST TECHNOLOGY**

<b>Engineering Test Coverage on Complex Sockets</b> .....	279
<i>M. J. Schneider, A. Shafi</i>	
<b>Solving In-Circuit Defect Coverage Holes with a Novel Boundary Scan Application</b> .....	288
<i>D. Dubberke, J. J. Grealish, B. V. Dick</i>	
<b>Augmenting Boundary-Scan Tests for Enhanced Defect Coverage</b> .....	297
<i>D. Norrgard, K. P. Parker</i>	

## **SESSION 12 SYSTEM-LEVEL MICROPROCESSOR ONLINE TEST**

<b>Low Energy On-Line SBST of Embedded Processors</b> .....	305
<i>A. Merentitis, N. Kranitis, A. Paschalis, D. Gizopoulos</i>	
<b>On-line Failure Detection in Memory Order Buffers</b> .....	315
<i>J. Carretero, X. Vera, P. Chaparro, J. Abella</i>	
<b>VAST: Virtualization-Assisted Concurrent Autonomous Self-Test</b> .....	325
<i>I. Hiroaki, Y. Li, S. Mitra</i>	

## **SESSION 13 POWER IMPACT ON COMPRESSION AND AT-SPEED SCAN**

<b>Reducing Power Supply Noise in Linear-Decompressor-Based Test Data Compression Environment for At-Speed Scan Testing</b> .....	335
<i>M. F. Wu, J. L. Huang, X. Wen, K. Miyase</i>	
<b>Low Power Scan Shift and Capture in the EDT Environment</b> .....	345
<i>D. Czysz, M. Kassab, X. Lin, G. Mrugalski, J. Rajski, J. Tyszer</i>	
<b>Frequency and Power Correlation between At-Speed Scan and Functional Tests</b> .....	355
<i>S. Sde-Paz, E. Salomon</i>	

## **SESSION 14 DIAGNOSTICS**

<b>Deterministic Diagnostic Pattern Generation (DDPG) for Compound Defects</b> .....	364
<i>F. Wang, Y. Hu, H. Li, X. Li, J. Ye, Y. Huang</i>	

<b>Diagnosis of design-silicon timing mismatch with feature encoding and importance ranking – the methodology explained</b> .....	374
<i>P. Bastani, N. Callegari, L. C. Wang, M. S. Abadir</i>	

<b>Efficiently Performing Yield Enhancements by Identifying Dominant Physical Root Cause from Test Fail Data</b> .....	384
<i>M. Sharma, B. Benware, L. Ling, D. Abercrombie, L. Lee, M. Keim, H. Tang, W. T. Cheng, T. P. Tai, Y. J. Chang, R. Lin, A. Man</i>	

## **SESSION 15 ACCESS AND OPENS AT BOARD TEST**

<b>Solder Bead on High Density Interconnect Printed Circuit Board</b> .....	393
<i>B. Chu</i>	
<b>Finding Power/Ground Defects on Connectors – Case Study</b> .....	398
<i>S. Hird, R. Weng</i>	

## **SESSIONS 16 INNOVATIVE SOLUTIONS TO COMPLEX SOCS**

<b>Architecture for Testing Multi-Voltage Domain SOC</b> .....	402
<i>L. Souef, C. Eychenne, E. Alié</i>	
<b>Integration of Hardware Assertions in Systems-on-Chip</b> .....	412
<i>J. Geuzebroek, B. Vermeulen</i>	
<b>Distributed Embedded Logic Analysis for Post-Silicon Validation of SOCs</b> .....	422
<i>H. F. Ko, A. B. Kinsman, N. Nicolici</i>	

## **SESSIONS 17 ADVANCES IN DIAGNOSIS**

<b>An Effective and Flexible Multiple Defect Diagnosis Methodology Using Error Propagation Analysis</b> .....	432
<i>X. Yu, R. D. Blanton</i>	
<b>Detection and Diagnosis of Static Scan Cell Internal Defect</b> .....	441
<i>R. Guo, L. Lai, Y. Huang, W. T. Cheng</i>	
<b>Optical Diagnostics for IBM POWER6 Microprocessor</b> .....	451
<i>P. Song, S. Ippolito, F. Stellari, J. Sylvestri, T. Diemoz, G. Smith, P. Muench, N. James, S. Kim, H. Saenz</i>	

## **SESSION 18 INDUSTRY EXPERIENCE WITH COMPLEX DESIGNS**

<b>Functional Test and Speed/Power Sorting of the IBM POWER6 and Z10 Processors</b> .....	460
<i>T. N. Pham, F. Clougherty, G. Salem, J. M. Crafts, J. Tetzloff, P. Moczygemba, T. M. Skergan</i>	
<b>Transition Test on UltraSPARC T2 Microprocessor</b> .....	467
<i>L. C. Chen, P. Dickinson, P. Mantri, M. Gala, P. Dahlgren, S. Bhattacharya, O. Caty, K. Woodling, T. Ziaja, D. Curwen, W. Yee, E. Su, G. Gu, T. Nguyen</i>	
<b>DFT Architecture for Automotive Microprocessors using On-Chip Scan Compression supporting Dual Vendor ATPG</b> .....	477
<i>H. Ahrens, R. Schlagenhaft, H. Lang, V. Srinivasan, E. Bruzzano</i>	

## **SESSION 19 POSTER PREVIEWS**

### **SESSION 20 RF TESTING**

<b>Octal-Site EVM Tests for WLAN Transceivers on “Very” Low-Cost ATE Platforms .....</b>	<b>487</b>
<i>G. Srinivasan, H. C. Chao, F. Taenzler</i>	
<b>Optimized EVM Testing for IEEE 802.11a/n RF ICs .....</b>	<b>496</b>
<i>E. Acar, S. Ozev, G. Srinivasan, F. Taenzler</i>	
<b>EVM Testing of Wireless OFDM Transceivers Using Intelligent Back-End Digital Signal Processing Algorithms .....</b>	<b>506</b>
<i>V. Natarajan, H. Choi, D. Lee, R. Senguttuvan, A. Chatterjee</i>	

### **SESSION 21 TEST QUALITY-DEFLECTS, DPPM AND PATTERNS, OH MY!**

<b>Towards a World Without Test Escapes: The Use of Volume Diagnosis to Improve Test Quality .....</b>	<b>516</b>
<i>S. Eichenbergera, J. Geuzebroekb, C. Horab, B. Kruseman, A. Majhi</i>	
<b>MODELING TEST ESCAPE RATE AS A FUNCTION OF MULTIPLE COVERAGES .....</b>	<b>526</b>
<i>K. M. Butler, J. M. Carulli, J. Saxena</i>	
<b>Evaluating the Effectiveness of Physically-Aware N-Detect Test using Real Silicon .....</b>	<b>535</b>
<i>Y. T. Lin, O. Poku, R. D. Blanton, P. Nigh, P. Lloyd, V. Iyengar</i>	

### **SESSION 22 SOFTWARE TO THE RESCUE!**

<b>A Method to Generate a Very Low Distortion, High Frequency Sine Waveform Using an AWG .....</b>	<b>544</b>
<i>A. Maeda</i>	
<b>Leveraging IEEE 1641 for Tester-Independent ATE Software .....</b>	<b>552</b>
<i>B. Van Wagenen, J. Vollmar, D. Thornton</i>	
<b>Bridging the gap between Design and Test Engineering for Functional Pattern Development .....</b>	<b>562</b>
<i>E. Aderholz, H. Ahrens, M. Rohleder</i>	

### **SESSION 23 “OUTSIDE THE BOX” DFT SOLUTIONS**

<b>“Plug &amp; Test” at System Level via Testable TLM Primitives .....</b>	<b>572</b>
<i>H. Alemzadeh, S. Di Carlo, F. Refan, P. Prinetto, Z. Navabi</i>	
<b>Design for Test of Asynchronous NULL Convention Logic (NCL) Circuits .....</b>	<b>582</b>
<i>W. K. Al-Assadi, S. Kakarla</i>	
<b>Non-contact Testing for SoC and RCP (SIPs) at Advanced Nodes .....</b>	<b>591</b>
<i>B. Moore, M. Mangrum, C. Sellathamby, M. Reja, T. Weng, B. Bai, E. Reid, I. Filanovsky, S. Slupsky</i>	

## **SESSION 24 SYSTEMS EFFECTS OF ERRORS AND PROTECTION METHODS**

<b>On the Correlation between Controller Faults and Instruction-Level Errors in Modern Microprocessors</b> .....	601
<i>N. Karimi, M. Maniatakos, A. Jas, Y. Makris</i>	
<b>Using Implications for Online Error Detection</b> .....	611
<i>K. Nepal, N. Alves, J. Dworak, R. I. Bahar</i>	
<b>A Field Analysis of System-level Effects of Soft Errors Occurring in Microprocessors used in Information Systems</b> .....	621
<i>S. Z. Shazli, M. Abdul-Aziz, M. B. Tahoori, D. R. Kaeli</i>	

## **SESSION 25 EMBEDDED MEMORY TEST**

<b>Direct Cell-Stability Test Techniques for an SRAM Macro with Asymmetric Cell-Bias-Voltage Modulation</b> .....	631
<i>A. Katayama, T. Yabe, O. Hirabayashi, Y. Takeyama, K. Kushida, T. Sasaki, N. Otsuka</i>	
<b>A Shared Parallel Built-In Self-Repair Scheme for Random Access Memories in SOCs</b> .....	638
<i>T. Tseng, J. Li</i>	
<b>Testing Methodology of Embedded DRAMs</b> .....	647
<i>C. Chang, M. C. T. Chao, R. F. Huang, D. Y. Chen</i>	

## **SESSION 26 RELIABILITY AND POWER SUPPLY NOISE ANALYSIS**

<b>Optimized Circuit Failure Prediction for Aging: Practicality and Promise</b> .....	656
<i>M. Agarwal, V. Balakrishnan, A. Bhuyan, K. Kim, B. C. Paul</i>	
<b>SoC Test Architecture Design and Optimization Considering Power Supply Noise Effects</b> .....	666
<i>F. Yuan, Q. Xu</i>	
<b>Observations of Supply-Voltage-Noise Dispersion in Sub-nsec</b> .....	675
<i>K. Takeuchi, G. Tanaka, H. Matsushita, K. Yoshizumi, Y. Katsuki, T. Sato</i>	

## **SESSION 27 ATE INSTRUMENTATION DESIGN IDEAS**

<b>A Hybrid A/D Converter with 120dB SNR and -125dB THD</b> .....	683
<i>M. Tamba</i>	
<b>Generating Test Signals for Noise-Based NPR/ACPR Type Tests in Production</b> .....	692
<i>S. Aouini, G. W. Roberts</i>	
<b>An Electronic Module for 12.8 Gbps Multiplexing and Loopback Test</b> .....	701
<i>D. C. Keezer, D. Minier, P. Ducharme, A. Majid</i>	

## **SESSION 28 PATH AND SMALL-DELAY FAULT ATPG**

<b>On Accelerating Path Delay Fault Simulation of Long Test Sequences</b> .....	710
<i>I. D. Huang, Y. S. Chang, S. Natarajan, R. Sharma, S. K. Gupta</i>	

<b>Implicit Identification of Non-Robustly Unsensitizable Paths using Bounded Delay Model</b> .....	719
<i>D. Jayaraman, E. Flanigan, S. Tragoudas</i>	
<b>Interconnect-Aware and Layout-Oriented Test-Pattern Selection for Small-Delay Defects</b> .....	729
<i>M. Yilmaz, K. Chakrabarty, M. Tehranipoor</i>	

## **SESSION 29 TEST STANDARDS 1**

<b>Boundary-Scan Testing of Power/Ground Pins</b> .....	739
<i>K. P. Parker, N. G. Jacobson</i>	
<b>IEEE 1500 Core Wrapper Optimization Techniques and Implementation</b> .....	747
<i>B. Mullane, M. Higgins, C. MacNamee</i>	
<b>Turbo1500: Toward Core-Based Design for Test and Diagnosis Using the IEEE 1500 Standard</b> .....	757
<i>L. T. Wang, R. Apte, S. Wu, B. Sheu, K. J. Lee, X. Wen, W. B. Jones, C. H. Yeh, W. S. Wang, H. J. Chao, J. Guo, J. Liu, Y. Niu, Y. C. Sung, C. C. Wang, F. Li</i>	

## **SESSION 30 TEST FOR PHYSICAL DEFECTS IN MEMORIES**

<b>Defect Oriented Testing of the Strap Problem Under Process Variations in DRAMs</b> .....	766
<i>Z. Al-Ars, S. Hamdioui, A. J. van de Goor, G. Mueller</i>	
<b>A New Wafer Level Latent Defect Screening Methodology for Highly Reliable DRAM Using a Response Surface Method</b> .....	776
<i>J. Nam, S. Chun, G. Koo, Y. Kim, B. Moon, J. Lim, J. Joo, S. Kang, H. Kim, K. Shin, K. Kang, S. Kang</i>	
<b>A High-Speed Structural Method for Testing Address Decoder Faults in Flash Memories</b> .....	786
<i>O. Ginez J. M. Portal, H. Aziza</i>	

## **SESSION 31 EMERGING TECHNOLOGIES TEST**

<b>Fabrication Defects and Fault Models for DNA Self-Assembled Nanoelectronics</b> .....	796
<i>V. Mao, C. Dwyer, K. Chakrabarty</i>	
<b>Built-in Self-Test and Fault Diagnosis for Lab-on-Chip Using Digital Microfluidic Logic Gates</b> .....	806
<i>Y. Zhao, T. Xu, K. Chakrabarty</i>	
<b>Testing Techniques for Hardware Security</b> .....	816
<i>M. Majzoobi, F. Koushanfar, M. Potkonjak</i>	

## **SESSION 32 DATA CONVERTER TESTING**

<b>Linearity Test Time Reduction for Analog-to-Digital Converters Using the Kalman Filter with Experimental Parameter Estimation</b> .....	826
<i>L. Jin</i>	
<b>Built-in Self-Calibration of On-chip DAC and ADC</b> .....	834
<i>W. Jiang, V. D. Agrawal</i>	



<b>A New Method for Measuring Aperture Jitter in ADC Output and Its Application to ENOB Testing</b> .....	844
<i>T. J. Yamaguchi, M. Kawabata, M. Soma, M. Ishida, K. Sawami, K. Uekusa</i>	

### **SESSION 33 TESTING FOR INTERCONNECT OPENS AND CROSSTALK**

<b>Test Generation for Interconnect Opens</b> .....	853
<i>X. Lin, J. Rajski</i>	
<b>A Novel Pattern Generation Framework for Inducing Maximum Crosstalk Effects on Delay-Sensitive Paths</b> .....	860
<i>J. Lee, M. Tehranipoor</i>	
<b>Extraction, Simulation and Test Generation for Interconnect Open Defects Based on Enhanced Aggressor-Victim Model</b> .....	870
<i>S. Hillebrecht, I. Polian, P. Engelke, B. Becker, M. Keim, W. T. Cheng</i>	

### **SESSION 34 TEST STANDARDS II**

<b>The Advantages of Limiting P1687 to a Restricted Subset</b> .....	880
<i>J. Doege, A. L. Crouch</i>	
<b>A New Language Approach for IJTAG</b> .....	888
<i>M. Portolan, S. Goyal, B. V. Treuren, C. H. Chiang, T. Chakraborty, T. B. Cook</i>	
<b>Problems Using Boundary-Scan for Memory Cluster Tests</b> .....	898
<i>B. G. Van Treuren, C. H. Chiang, K. Honaker</i>	

### **SESSION 35 SCAN-BASED COMPRESSION AND TRANSITION TESTS**

<b>Increasing Scan Compression by Using X-Chains</b> .....	908
<i>P. Wohl, J. A. Waicukauski, F. Neuveux</i>	
<b>Align-Encode: Improving the Encoding Capability of Test Stimulus Decompressors</b> .....	918
<i>O. Sinanoglu</i>	
<b>Launch-on-Shift-Capture Transition Tests</b> .....	928
<i>I. Park, E. J. McCluskey</i>	
<b>A Tutorial on STDF Fail Datalog Standard</b> .....	937
<i>A. Khoche, P. Burlison, J. Rowe, G. Plowman</i>	
<b>Parametric Testing of Optical Interfaces</b> .....	947
<i>B. Achkir, P. Zivny, B. Eklow</i>	
<b>Justifying DFT with a Hierarchical Top-Down Cost-Benefit Model</b> .....	948
<i>S. Davidson</i>	
<b>The Economics of Harm Prevention through Design for Testability</b> .....	958
<i>L. Y. Ungar</i>	
<b>On-chip Timing Uncertainty Measurements on IBM Microprocessors</b> .....	966
<i>R. Franch, P. Restle, N. James, W. Huott, J. Friedrich, R. Dixon, S. Weitzel, K. Van Goor, G. Salem</i>	
<b>Jitter and Signal Integrity Verification for Synchronous and Asynchronous I/Os at Multiple to 10 GHz/Gbps</b> .....	973
<i>M. P. Li</i>	

<b>Jitters in high performance microprocessors</b> .....	979
<i>T. M. Mak</i>	
<b>Beyond 10 Gbps? Challenges of Characterizing Future I/O Interfaces with Automated Test Equipment</b> .....	985
<i>J. Moreira, H. Barnes, H. Kaga, M. Comai, B. Roth, M. Culver</i>	
<b>Embedded Testing in an In-Circuit Test Environment</b> .....	995
<i>J. Malian, B. Eklow</i>	
<b>Hardware-based Error Rate Testing of Digital Baseband Communication Systems</b> .....	1001
<i>A. Alimohammad, S. F. Fard, B. F. Cockburn</i>	
<b>Power-Aware DFT – Do we really need it?</b> .....	1011
<i>N. Mukherjee</i>	
<b>Power-Aware DFT – Do we really need it?</b> .....	1012
<i>P. Krishnamurthy</i>	
<b>Power-Aware DFT – Do Not Risk It, Use It</b> .....	1013
<i>B. Pouya</i>	
<b>Some Burning Issues that Justify Power-Aware DFT</b> .....	1014
<i>J. Rearick</i>	
<b>Analog Test Technology: Stable and Grounded, or Open Loop and Spurious?</b> .....	1015
<i>M. Purtell</i>	
<b>Analog Test Technology: Stable and Grounded, or Open Loop and Spurious</b> .....	1016
<i>S. Goyal</i>	
<b>Analog Test Technology: Challenges Abound</b> .....	1017
<i>T. J. Anderson</i>	
<b>Analog &amp; Mixed-Signal are Key for Test Development Engineering Program</b> .....	1018
<i>T. I. Schmitz</i>	
<b>Will Test Compression Run Out of Gas?</b> .....	1019
<i>S. K. Goel, E. J. Marinissen</i>	
<b>Will Test Compression Run Out of Gas?</b> .....	1020
<i>S. Bhatia</i>	
<b>Will Test Compression Run Out Of Gas?</b> .....	1021
<i>S. Pateras</i>	
<b>We Need Faster &amp; Deeper Scan and More Realistic Tests</b> .....	1022
<i>J. Rivoir, S. Architect</i>	
<b>The Limits of Compression</b> .....	1024
<i>T. W. Williams</i>	
<b>Debug War Stories</b> .....	1026
<i>L. Winenberg</i>	
<b>Debug War Stories</b> .....	1027
<i>D. Carder</i>	
<b>Yield Learning: Everybody Gains, But Who Picks up the Tab?</b> .....	1028
<i>P. Burlison</i>	
<b>The University DFT Tool Showdown - Introduction</b> .....	1029
<i>S. Davidson</i>	
<b>Overview of OpenSPARC</b> .....	1030
<i>I. Parulkar</i>	

<b>Functional test-bench refinement through automatic constraint extraction .....</b>	<b>1031</b>
<i>L. C. Wang, O. Guzey</i>	
<b>Benchmarking Academic DFT Tools on the OpenSparc Microprocessor .....</b>	<b>1032</b>
<i>I. Polian</i>	
<b>On the generation of test programs for chip multi-thread computer architectures.....</b>	<b>1033</b>
<i>D. Ravotto, E. Sanchez, M. S. Reorda, G. Squillero</i>	
<b>Challenges in Scaling Software-Based Self-Testing to Multithreaded Chip Multiprocessors.....</b>	<b>1034</b>
<i>D. Gizopoulos</i>	
<b>Overview of IEEE P1450.6.2 Standard Creating CTL Model For Memory Test and Repair .....</b>	<b>1036</b>
<i>N/A</i>	
<b>IEEE P1581 drastically simplifies connectivity test for memory devices .....</b>	<b>1037</b>
<i>Heiko Ehrenberg</i>	
<b>LOW POWER TEST .....</b>	<b>1038</b>
<i>S. Bahl, R. Sarkar, A. Garg</i>	
<b>IEEE 1500 Compatible Secure Test Wrapper For Embedded IP Cores.....</b>	<b>1039</b>
<i>G. Chiu, J. C. Li</i>	
<b>Test-Access Solutions for Three-Dimensional SOCs.....</b>	<b>1040</b>
<i>X. Wu, Y. Chen, K. Chakrabarty, Y. Xie</i>	
<b>SOC Test Optimization with Compression-Technique Selection .....</b>	<b>1041</b>
<i>A. Larsson, X. Zhang, E. Larsson, K. Chakrabarty</i>	
<b>SoC Yield Improvement: Redundant Architectures to the Rescue? .....</b>	<b>1042</b>
<i>J. Vial, A. Bosio, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel</i>	
<b>Platform Independent Test Access Port Architecture .....</b>	<b>1043</b>
<i>A. Margulis, D. Akselrod, T. Wood, S. Metsis</i>	
<b>NoC Reconfiguration for Utilizing the Largest Fault-free Connected Sub-structure.....</b>	<b>1044</b>
<i>A. Alaghi, M. Sedghi, N. Karimi, Z. Navabi</i>	
<b>VLSI Test Exercise Courses for Students in EE Department .....</b>	<b>1045</b>
<i>S. Komatsu</i>	
<b>Hardware Overhead Reduction for Memory BIST .....</b>	<b>1046</b>
<i>M. Arai, K. Iwasaki, M. Nakao, I. Suzuki</i>	
<b>A Low-Cost Programmable Memory BIST Design for Multiple Memory Instances.....</b>	<b>1047</b>
<i>C. Lin, C. Huang, D. Lu, C. Hsu, W. T. Chiu, Y. Chen, Y. Chang</i>	
<b>The Importance of Functional-Like Access for Memory Test .....</b>	<b>1048</b>
<i>J. Phelps, C. Johnson, C. Goodrich, A. Kokrady</i>	
<b>An Efficient Secure Scan Design for an SoC Embedding AES Core.....</b>	<b>1049</b>
<i>J. Song, T. Jung, J. Lee, H. Jeong, B. Kim, S. Park</i>	
<b>Diagnosis of Mask-Effect Multiple Timing Faults in Scan Chains .....</b>	<b>1050</b>
<i>J. Ye, F. Wang, Y. Hu, X. Li</i>	
<b>Diagnosis of Logic-to-chain Bridging Faults.....</b>	<b>1051</b>
<i>W. Liu, W. Tsai, H. Lin, J. C. Li</i>	
<b>Power Distribution Failure Analysis Using Transition-Delay Fault Patterns .....</b>	<b>1052</b>
<i>J. Ma, J. Lee, M. Tehranipoor</i>	
<b>Is It Cost-Effective to Achieve Very High Fault Coverage for Testing Homogeneous SoCs with Core-Level Redundancy?.....</b>	<b>1053</b>
<i>L. Huang, Q. Xu</i>	

<b>System JTAG Initiative Group Advancements</b> .....	1054
<i>B. G. Van Treuren</i>	
<b>A Generic Framework for Scan Capture Power Reduction in Test Compression Environment</b> .....	1055
<i>X. Liu, F. Yuan, Q. Xu</i>	
<b>High Test Quality in Low Pin Count Applications</b> .....	1056
<i>J. D'Souza, S. Mahadevan, N. Mukherjee, G. Rhodes, J. Moreau, T. Droniou, P. Armagnat, D. Sartoretti</i>	
<b>Capture and Shift Toggle Reduction (CASTR) ATPG to Minimize Peak Power Supply Noise</b> .....	1057
<i>H. Lin, J. Wen, J. Li, M. Chang, M. Tsai, S. Huang, C. Tseng</i>	
<b>Test Quality Improvement with Timing-aware ATPG: Screening small delay defect case study</b> .....	1058
<i>C. J. Chang, T. Kobayashi</i>	
<b>FPGA Time Measurement Module: Preliminary Results</b> .....	1059
<i>W. J. Bowhars</i>	
<b>Wireless Test Structure for Integrated Systems</b> .....	1060
<i>Z. Noun, P. Cauvet, M. Flottes, D. Andreu, S. Bernard</i>	
<b>Overview of a High Speed Top Side Socket Solution</b> .....	1061
<i>J. Stewart, T. Animashaun</i>	
<b>Improving the Accuracy of Test Compaction through Adaptive Test Update</b> .....	1062
<i>S. Biswas, R. D. Blanton</i>	

*Author Index*