2009 IEEE VLSI Test Symposium
(VTS)

Santa Cruz, California, USA
03 – 07 May 2009
# TABLE OF CONTENTS

## SESSION 1

### SESSION 1A: MICROPROCESSOR TEST

**Efficient Array Characterization in the UltraSPARC T2** ................................................................. 1  
*Thomas Ziaja, P.J. Tan*

**Instruction-Level Impact Comparison of RT- vs. Gate-Level Faults in a Modern Microprocessor Controller** ............................................................................................................................... 7  
*Mihail Maniatakos, Naghmeh Karimi, Chandra Tirumurti, Abhijit Jas, Yiorgos Makris*

**Modeling and Testing Comparison Faults of TCAMs with Asymmetric Cells** ................................. 13  
*Yong-Jyun Hu, Yu-Jen Huang, Jin-Fu Li*

### SESSION 1B: FAULT MODELS

**An Electrical Model for the Fault Simulation of Small Delay Faults Caused by Crosstalk Aggravated Resistive Short Defects** ................................................................................................................. 19  
*N. Houarche, M. Comte, M. Renovell, A. Czutro, P. Engelke, I. Polian, B. Becker*

**Small Delay Fault Model for Intra-Gate Resistive Open Defects** ...................................................... 25  
*Masayuki Arai, Akifumi Suto, Kazuhiko Iwasaki, Katsuyuki Nakano, Michihiro Shintani, Kazumi Hatayama, Takashi Aikyo*

**Defect Detection Differences between Launch-Off-Shift and Launch-Off-Capture in Sense-Amplifier-Based Flip-Flop Testing** .................................................................................................................. 31  
*Haluk Konuk*

## SESSION 2

### SESSION 2A: ROBUST DESIGN AND FAULT TOLERANCE

**Soft-Error Hardening Designs of Nanoscale CMOS Latches** ................................................................. 37  
*Sheng Lin, Yong-Bin Kim, Fabrizio Lombardi*

**Exploiting Unused Spare Columns to Improve Memory ECC** .............................................................. 43  
*Rudrajit Datta, Nur A. Touba*

**An Adaptive-Rate Error Correction Scheme for NAND Flash Memory** ............................................. 49  
*Te-Hsuan Chen, Yu-Ying Hsiao, Yu-Tsao Hsing, Cheng-Wen Wu*

### SESSION 2B: DELAY FAULT TESTING I

**Compact Delay Test Generation with a Realistic Low Cost Fault Coverage Metric** ........................... 55  
*Zheng Wang, Duncan M.H. Walker*

**Recursive Path Selection for Delay Fault Testing** ................................................................................. 61  
*Jaeyoung Chung, Jacob A. Abraham*
A Synthesis Method to Alleviate Over-Testing of Delay Faults Based on RTL Don't Care Path Identification ................................................................. Yuki Yoshikawa, Satoshi Ohtake, Tomoo Inoue, Hideo Fujiwara

SESSION 3

SESSION 3A: DEBUG

Automated Selection of Signals to Observe for Efficient Silicon Debug .............................................................. Joon-Sung Yang, Nur A. Touba

A New Post-Silicon Debug Approach Based on Suspect Window ................................................................. Jianliang Gao, Yinhe Han, Xiaowei Li

Automated Debug of Speed Path Failures Using Functional Tests .............................................................. Richard McLaughlin, Srikanth Venkataraman, Carlston Lim

SESSION 3B: DELAY FAULT TESTING II

Output Hazard-Free Transition Delay Fault Test Generation ................................................................. Sreekumar Menon, Adit D. Singh, Vishwani Agrawal

Efficient Scheduling of Path Delay Tests for Latch-Based Circuits ................................................................. Kun Young Chung, Sandeep K. Gupta

Effective and Efficient Test Pattern Generation for Small Delay Defect .......................................................... Sandeep Kumar Goel, Narendra Devta-Prasanna, Ritesh P. Turakhia

SESSION 4

Special Session 4A: Panel: Apprentice - VTS Edition: Season 2 ................................................................. Kee Sup Kim

Special Session 4B: Panel: DFT and Test Problems from the Trenches ................................................................. Haluk Konuk

SESSION 5

SESSION 5A: DIAGNOSIS

Multiple-Fault Diagnosis Using Faulty-Region Identification ................................................................. Megn-Jai Tasi, Mango C.T. Chao, Jing-Yang Jou, Meng-Chen Wu

Predictive Test Technique for Diagnosis of RF CMOS Receivers ................................................................. K. Suenaga, S. Bota, R. Picos, E. Isern, M. Roca, E Garcia-Moreno

Controlling DPPM through Volume Diagnosis ................................................................. Xiaochun Yu, Yen-Tzu Lin, Wing-Chiu Tam, Osei Poku, R.D. Blanton

SESSION 5B: DELAY FAULT TESTING AND SIGNAL INTEGRITY

Scalable Compact Test Pattern Generation for Path Delay Faults Based on Functions ................................ Edward Flanigan, Spyros Tragoudas, Arkan Abdulrahman
The ATPG Conflict-Driven Scheme for High Transition Fault Coverage and Low Test Cost ................................................................. 136
Zhen Chen, Dong Xiang, Boxue Yin

A High-Level Signal Integrity Fault Model and Test Methodology for Long On-Chip Interconnections ................................................................. 142
Sunghoon Chun, Yongjoon Kim, Taejin Kim, Sungho Kang

SESSION 6

SESSION 6A: YIELD

False Path Aware Timing Yield Estimation under Variability ................................................................. 148
Lin Xie, Azadeh Davoodi, Kewal K. Saluja, Abhishek Sinkar

Bridging DFM Analysis and Volume Diagnostics for Yield Learning - A Case Study ........................................... 154
Ritesh Turakhia, Mark Ward, Sandeep Kuma Goel, Brady Benware

Yield and Cost Analysis of a Reliable NoC ........................................................................................................... 160
Saeed Shamshiri, Kwang-Ting Cheng

SESSION 6B: BIST

Restrict Encoding for Mixed-Mode BIST ........................................................................................................... 166
Abdul-Wahid Hakmi, Stefan Holst, Hans-Joachim Wunderlich, Jürgen Schlöffel, Friedrich Hapke, Andreas Glowatz

A Scalable, Digital BIST Circuit for Measurement and Compensation of Static Phase Offset ........................................................................................................... 172
Keith A. Jenkins, Lionel Li

Experimental Validation of a BIST Technique for CMOS Active Pixel Sensors ........................................... 176
Livier Lizarraga, Salvador Mir, Gilles Sicard

SESSION 7

SESSION 7A: TEST AND VERIFICATION

Physically-Aware N-Detect Test Relaxation ........................................................................................................... 182
Yen-Tzu Lin, Chukwuemeka U. Ezekwe, R. D. Blanton

Automatic Selection of Internal Observation Signals for Design Verification ........................................... 188
Tao Lv, Hua-wei Li, Xiao-wei Li

STDF Memory Fail Datalog Standard ........................................................................................................... 194
Ajay Khoche, Jay Katz, Sauro Landini, Kochen Liao, Neetu Agrawal, Glenn Plowman, Song-lin Zuo, Liyang Lai, John Rowe, Thomas Zanon

SESSION 7B: TRANSISTOR AGING AND POWER SUPPLY NOISE

Testing for Transistor Aging ......................................................................................................................... 200
Altug Hakan Baba, Subhasish Mitra
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>SESSION 8: New Topics: At-Speed Testing in the Face of Process Variations</td>
<td>Bernard Courtois, Chantu Viswesvariah</td>
</tr>
<tr>
<td>10</td>
<td>SESSION 10A: TEST COMPACTION</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Highly X-Tolerant Selective Compaction of Test Responses</td>
<td>Grzegorz Mrugalski, Nilanjan Mukherjee, Janusz Rajski, Dariusz Czysz, Jerzy Tyszer</td>
</tr>
<tr>
<td></td>
<td>Dynamic Test Compaction for Transition Faults in Broadside Scan Testing Based on an Influence Cone Measure</td>
<td>Dong Xiang, Boxue Yin, Kwang-Ting Cheng</td>
</tr>
<tr>
<td></td>
<td>Maintaining Accuracy of Test Compaction through Adaptive Re-learning</td>
<td>Sounil Biswas, R. D. Blanton</td>
</tr>
<tr>
<td></td>
<td>SESSION 10B: TEST AND RADIATION TEST</td>
<td></td>
</tr>
<tr>
<td></td>
<td>RT-Level Deviation-Based Grading of Functional Test Sequences</td>
<td>Hongxia Fang, Krishnendu Chakrabarty, Abhijit Jas, Srinivas Putil, Chandra Tirumurti</td>
</tr>
<tr>
<td></td>
<td>Analytical Model for Multi-site Efficiency with Parallel to Serial Test Times, Yield and Clustering</td>
<td>Naveen Velamati, Robert Daasch</td>
</tr>
</tbody>
</table>
SESSION 11

SESSION 11A: ANALOG TEST AND CALIBRATION

On-Line Calibration and Power Optimization of RF Systems Using a Built-In Detector
Chaoming Zhang, Ranjit Gharpurey, Jacob A. Abraham

Calibration and Testing Time Reduction Techniques for a Digitally-Calibrated Pipelined ADC
Hsiu-Ming Chang, Chin-Hsuan Chen, Kuan-Yu Lin, Kwang-Ting Cheng

A Time Domain Method to Measure Oscillator Phase Noise
Kenneth Blakkan, Mani Soma

A Packet Based 2x-Site Test Solution for GSM Transceivers with Limited Tester Resources
Erdem Serkan Erdogan, Sule Ozev

SESSION 11B: EMERGENT TECHNOLOGY AND SECURITY

Design-for-Testability for Digital Microfluidic Biochips
Tao Xu, Krishnendu Chakrabarty

Stuck-Open Fault Leakage and Testing in Nanometer Technologies
Julio Vazquez, Victor Champac, Chuck Hawkins, Jaume Segura

SS-KTC: A High-Testability Low-Overhead Scan Architecture with Multi-level Security Integration
Unni Chandran, Dan Zhao

Characterization of Effective Laser Spots during Attacks in the Configuration of a Virtex-II FPGA
Gaetan Canivet, Regis Leveugle, Jessy Clediere, Frederic Valette, Marc Renaudin

Special Session 11C: Embedded Tutorial: System-on-a-Chip Power Management Implications on Validation and Testing
Bhanu Kapoor

SESSION 12

Special Session 12A: Panel: Analog Characterization and Test: The Long Road to Realization
Arani Sinha, Amitava Majumdar, Vasu Ganti

Special Session 12B: Panel: Functional Verification Planning and Management - Are Good Intentions Good Enough?
Andrew Piziali

Author Index