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T.Garibay, R.Reis;  
*Austin Design Center Wireless Terminals Business Unit Texas Instruments, USA

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H.-L.Chen, J.-S.Chiang;  
+Tamkang University, Tamsui, Taipei, Taiwan

Invited Paper: Implementation and Evaluation of Fine-grain Run-time Power Gating for a Multiplier  
K.Usami*, M.Nakata*, T.Shirai†, S.Takeda‡, N.Seki‡, H.Amano‡, H.Nakamura‡;  
*Shibaura Institute of Technology, Tokyo, Japan  
†Keio University, Yokohama, Japan  
‡The University of Tokyo, Tokyo, Japan

Improvement of LDO’s PSRR Deteriorated By Reducing Power Consumption: Implementation and Experimental Results  
S.Heng, C.-K.Pham;  
*University of Electro-Communications, Choufu, Tokyo, Japan

Large Random Telegraph Noise in Sub-Threshold Operation of Nano-Scale nMOSFETs  
*Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD, USA  
†Department of Electrical and Computer Engineering, Rutgers University, Piscataway, NJ, USA  
§TSMC Ltd., Hsin-Chu, Taiwan, R.O.C.

Session B  ESD

Invited Paper: Low-Leakage Electrostatic Discharge Protection Circuit in 65-nm Fully-Silicided CMOS Technology  
*Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C.  
+United Microelectronics Corporation, Hsinchu, Taiwan

Invited Paper: ESD Protection for RF/AMS ICs: Design and Optimization  
*Dept. of Electrical Engineering, University of California, Riverside, CA, USA  
‡Skyworks Solutions, Inc., Irvine, CA, USA  
§SMIC, China  
%;Tsinghua University, China
A 0.9 V to 5 V Mixed-Voltage I/O Buffer Using NMOS Clamping Technique
C.-C.Wang, J.-W.Liu, R.-C.Kuo;
National Sun Yat-Sen University, Department of Electrical Engineering, Kaohsiung, Taiwan

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M.Germain, J.Derluyn, M.van Hove, S.Degroote, J.Das, K.Cheng, G.Borghs;
IMEC, Leuven, Belgium

Invited Paper: Recent Advances in RF-LDMOS High-Power IC Development
W.R.Burger;
RF Division, RF, Analog, and Sensors Group, Freescale Semiconductor, Tempe, AZ, USA

Through Silicon Via Stress Characterization
T.Dao*, D.H.Triyoso*, M.Petras+, M.Canonico;
*Freescale Semiconductor, Austin, Texas, USA
+Zarlink Semiconductor, Austin, TX, USA

A 30V Complementary Bipolar Technology for xDSL Line Drivers
C.J.Speyer*, T.J.Krutsick+, J.K.Moriart*;
*Zarlink Semiconductor, Austin, TX, USA
+Zarlink Semiconductor, Reading, PA, USA

Session D  CAD
Cell Merge: A Basic-Pre-Clustering Clustering Algorithm for Placement
X.Zhang, T.Takeuchi, M.Toyonaga;
Faculty of Science, Kochi University, Kochi, Japan

AKEBONO: A Novel Quick Incremental Placer
X.Zhang, T.Takeuchi, M.Toyonaga;
Faculty of Science, Kochi University, Kochi, Japan

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N.Nemade, A.Sprintson, J.Hu;
Texas A&M University, College Station, Texas, USA

Timing Analysis of Dual-Edge-Triggered Flip-Flop Based Circuits with Clock Gating
C.Oh, S.Kim, Y.Shin;
Department of Electrical Engineering, KAIST, Daejeon, Korea

Timing Yield Estimation with Clock Network Correlations by Propagating Discrete Probability Distributions
*Department of Electrical Engineering, KAIST, Daejeon, Korea
+Department of Electrical Engineering, National Tsing Hua University, Hsinchu, Taiwan
Network Flow Based BSM Assignment
H.Xiang*, H.Ren*, T.Zhou+
*IBM T.J. Watson Research Center, Yorktown Heights, NY, USA
+IBM System & Technology Group, USA

A Simple Fast Exact Density Calculation Algorithm
H.Xiang*, C.Chu+, R.Puri+
*IBM T.J. Watson Research Center, Yorktown Heights, NY, USA
+Iowa State University, Ames IA, USA

Accurate Global & Local circuit leakage current analysis based on Design of Experiment method
M.Yap San Min, O.Thomas, A.Valentian, F.de Crécy;
CEA, LETI, MINATEC, Grenoble, France

Session E  PID/High-K

Invited Paper: The Negative Bias Temperature Instability vs. High-Field Stress Paradigm
*Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD, USA +TSMC Ltd., Hsin-Chu, Taiwan, R.O.C.

Invited Paper: Unified TDDB Model for Stacked High-k Dielectrics
B.H.Lee;
Nanosystems Engineering and the department of Material Science and Engineering at Gwangju Institute of Science and Technology, Gwangju, Korea

Factors impacting stabilization of tetragonal phase in HfxZr1-xO2 high-k dielectrics
D.H.Triyoso, R.I.Hegde, R.Gregory, G.Spencer, J.K.Schaeffer, M.Raymond;
Technology Solutions Organization, Freescale Semiconductor Inc., Austin, TX, USA

Impact of Gate-Oxide Breakdown on Power-Gated SRAM
H.-I.Yang, C.-T.Chuang, W.Hwang;
Department of Electronics Engineering & Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R. O. C.

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A.Matsuda, Y.Nakakubo, R.Ogino, H.Ohta, K.Eriguchi, K.Ono;
Graduate School of Engineering, Kyoto University, Sakyoku, Kyoto, Japan

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K.Eriguchi, A.Matsuda, Y.Nakakubo, M.Kamei, H.Ohta, K.Ono;
Kyoto University, Yoshida-Honmachi, Sakyoku, Kyoto, Japan

Session F  SER

Invited Paper: SEE Characterization and Mitigation in Ultra-Deep Submicron

*Aix-Marseille University, CNRS, University Institute of France (IUF) and Institut Carnot STAR (IC-STAR, Marseille), Institute of Materials, Microelectronics and Nanosciences of Provence (IM2NP, UMR CNRS 6242), Bâtiment IRPHE, Marseille, France
+STMicroelectronics, Crolles Cedex, France
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%Laboratoire Souterrain de Modane (LSM, CEA-CNRS), Modane, France
$JB R&D, Ferrière, Saint-Etienne en Dévoluy, France
£Laboratory of Nuclear Problems, JINR, Dubna, Moscow region, Russia

A 2.5 GHz Radiation Hard Fully Self-biased PLL using 0.25 μm SOS-CMOS Technology

P.P.Ghosh, E.Xiao;
Electrical Engineering Department, University of Texas at Arlington, TX, USA

Soft Error Estimates for Fabless Companies

A.Dixit, R.Heald;
Sun Microsystems, Santa Clara, CA, USA

Session G  System on a Chip

Invited Paper: A Low-Power Multi-Core Media Co-Processor for Mobile Application Processors

*Digital Media SoC Dept., Center for Semiconductor Research and Development, Toshiba Corporation, Kawasaki, Japan
+Advanced Circuit Design Dept., Center for Semiconductor Research and Development, Toshiba Corporation, Kawasaki, Japan

Implementation of Area Efficient H.264/AVC CAVLC Decoder

B.-S.Choi, J.-Y.Lee;
Chonbuk University, SoC Lab. 7th Engineering Department, Jeon-ju, Korea, South (Republic of)

Implementation of Scalable Interconnect Networks for data reordering used in Discrete Trigonometric Transforms (DTT)

A.Hussein*, A.Suleiman*, N.Kerkiz*, D.Akopian*;
*University of Texas at San Antonio, Electrical and Computer Engineering Department, USA
+Intel Corporation, Austin, Texas, USA
Semi-Custom Design Flow: Leveraging Place and Route Tools in Custom Circuit Design

N.N. Eleyan, K. Lin, M. Kamal, B. Mohammad, P. Bassett;
Qualcomm, DSP Core Design, Austin, TX, USA

Invited Paper: Technology and Design Aspects of Ultra-Thin Silicon Chips for Bendable Electronics

Institute for Microelectronics, Stuttgart, Germany

Session H  Advance Transistors

Invited Paper: The Tunnel Source MOSFET: A Novel Asymmetric Device Solution for Ultra-Low Power Applications

V. Nagavarapu, A. Tura, R. Jhaveri, H.-Y. Chang, J. Woo;
UCLA CMOS Laboratory, University of Los Angeles, Los Angeles, CA, USA

Invited Paper: High mobility III-V Channel MOSFETs for Post-Si CMOS Applications

*IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA
+IBM Zürich Research Laboratory, Rüschlikon, Switzerland
#Electrical Engineering, Princeton University, Princeton, NJ, USA

Systematic Approach of FinFET based SRAM Bitcell Design for 32nm Node and Below

*Qualcomm Incorporated, San Diego, CA, USA
+Electrical Engineering Dept., University of California, Berkeley, CA, USA

Stacked 3-Dimensional 6T SRAM Cell with Independent Double Gate Transistors

*Technische Universität München, Germany
+Warsaw University of Technology, Poland
#Carnegie Mellon University, Pittsburgh, USA

Dynamic Power Analysis for Custom Designs

S. Bijansky, B. Mohd, B. Mohammad;
Qualcomm, Austin, Texas, USA

A Novel Poly-Si Thin-Film Transistor with Multi-Trenched Body by Using Isotropic-etching for Suppressing Off-State Leakage

Department of Electrical Engineering, National, Sun Yat-Sen University, Kaohsiung, Taiwan, R.O.C.

Future of Planar Self-Aligned Block Oxide Based MOSFET Technology

Department of Electrical Engineering, National, Sun Yat-Sen University, Kaohsiung, Taiwan, R.O.C.
Session I  Memory

Invited Paper: Embedded Nonvolatile Memory Technology

K. Baker;
Freescale Semiconductor, Austin, TX, USA

Robust Multi-VT 4T SRAM Cell in 45nm Thin BOX Fully-Depleted SOI technology with Ground Plane

J.-P. Noel*, O. Thomas*, C. Fenouillet-Beranger*, M.-A. Jaud*, A. Amara*;
*CEA, LETI, MINATEC, Grenoble, France
+ISEP, Paris, France

Compact 6T SRAM cell with robust Read/Write stabilizing design in 45nm Monolithic 3D IC technology

O. Thomas, M. Vinet, O. Rozeau, P. Batude, A. Valentian;
CEA/LETI-MINATEC, Grenoble, France

Operation of Multi-Level Phase Change Memory Using Various Programming Techniques

*Department of Electronic Engineering, National Ilan University, Taiwan, ROC
+Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University, Taiwan, ROC

Session J  DFM/DFT/DFR/DFY


F. Klass, A. Jain, G. Hess;
Apple Inc., Cupertino, CA, USA

Invited Paper: Statistical-aware Designs for the nm Era

R. Joshi*, R. Kanj**;
*IBM TJ Watson Research Center, Yorktown Heights, NY, USA
**IBM Austin Research Labs, Austin, Texas, USA

Dynamic Cache Resizing Architecture for High Yield SOC

B. Mohammad*, M. T. Rab**, Kh. Mohammad*, M. A. Suleman**;
*Qualcomm Incorporated, USA
**University of Texas at San Antonio, USA

An Innovative Timing Slack Monitor for Variation Tolerant Circuits

*CEA, LETI, MINATEC, Grenoble, France
+LIRMM - CNRS - Université Montpellier II, Montpellier, France

Machine Learning based Lithographic Hotspot Detection with Critical-Feature Extraction and Classification

D. Ding, X. Wu, J. Ghosh, D. Z. Pan;
ECE Dept. Univ. of Texas at Austin, Austin, TX, USA
Session K  Emerging Technology

Invited Paper: Monolayer Doping and Diameter-Dependent Electron Mobility Assessment of Nanowires
A.C.Ford*, J.C.Ho*, Y.-L.Chueh*, A.Javey*;*
*Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA, USA
+Lawrence Berkeley National Laboratory and Berkeley Sensor and Actuator Center, University of California, Berkeley, CA, USA

Invited Paper: Self-aligned In0.53Ga0.47As MOSFETs with Atomic Layer Deposited Al2O3, ZrO2, and Stacked Al2O3/ZrO2 Gate Dielectrics
H.Zhao, J.C.Lee;
University of Texas at Austin, Austin, TX, USA

One-Transistor Bistable-Body Tunnel SRAM
K.Karda, J.Brockman, S.Sutar, A.Seabaugh, J.Nahas;
University of Notre Dame, Notre Dame, IN, USA

Complementary Nano-Electro-Mechanical Switches For Ultra-Low-Power Applications: Fabrication, Design and Simulation
K.Alzoubi*, D.G.Saab*, M.Tabib-Azar+;
*Department of EECS, Case Western Reserve University, Cleveland, Ohio, USA
+Department of ECE, University of Utah, Salt Lake City, Utah, USA

Session L  RF/Analog

A 1.8V 200mW 8-bit 1GSPS CMOS A/D Converter with a Cascaded-Folding and an Interpolation
J.Hwang, D.Lee, S.Park, J.Moon, M.Song;
Dept. of Semiconductor Science, Dongguk University, Seoul, Korea

An 8-bit 500MHz Two-Step ADC in 0.13-um SiGe BiCMOS
P.-H.Chen, M.Peckerar;
Analog and Mixed-signal Systems Design Laboratory, University of Maryland, College Park, MD, USA

Hot Carrier Stress Effect on the Performance of 65 nm CMOS Low Noise Amplifier
Y.Shen, J.Lee, H.Shin;
Inter-University Semiconductor Research Center (ISRC) and School of Electrical Engineering, Seoul National, University, Kwanak-gu, Seoul, Korea

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