2009 IEEE International High Level Design Validation and Test Workshop

(HLDVT 2009)

San Francisco, California, USA
4 – 6 November 2009
TABLE OF CONTENTS

Session 1: Verification Methodologies and Applications

Analysis of Scheduled Latency Insensitive Systems with Periodic Clock Calculus ............................................................... 1
Bin Xue and Sandeep Shukla—Virginia Tech, U.S.A.

Exploiting Hierarchical Encodings of Equality to Design Independent Strategies in Parallel SMT Decision Procedures for a Logic of Equality ................................................................. 8
Miroslav N. Velev and Ping Gao—Aries Design Automation, LLC, U.S.A.

FLARE: A Design Environment for FLASH-Based Space Applications ................................................................................ 14
Maurizio Caramia—Thales Alenia Space Italia, Italy; Stefano Di Carlo, Michele Fabiano and Paolo Prinetto—Politecnico di Torino, Italy

MCBCG: Model Checking Based Sequential Clock-Gating ................................................................................................ 20
Sumit Ahuja and Sandeep Shukla—Virginia Tech, U.S.A.

Session 2: Invited Session—RTL Validation and Debug

Automated Debugging with High Level Abstraction and Refinement .................................................................................. 26
Sean Safarpour—Vennsa Technologies Inc., Canada; Andreas Veneris—University of Toronto, Canada

STAR: Generating Input Vectors for Design Validation by Static Analysis of RTL ............................................................... 32
Lingyi Liu and Shobha Vasudevan—University of Illinois at Urbana-Champaign, U.S.A.

Session 3: Formal Methods for Verification

Learning from Constraints for Formal Property Checking ......................................................................................... 38
In-Ho Moon and Kevin Harer—Synopsys Inc., U.S.A.

Exploiting Incrementality in SAT-Based Search for Multiple Equivalence-Preserving Transformations in Combinational Circuits .................................................................................................. 46
Gianpiero Cabodi, Leandro Dipietro, Marco Murciano and Sergio Nocco—Politecnico di Torino, Italy

PowerRanger: Assessing Circuit Vulnerability to Power Attacks Using SAT-Based Static Analysis ................................ 54
Jeff Hao and Valeria Bertacco—University of Michigan at Ann Arbor, U.S.A.

Session 4: Panel—SystemC Why: To Design or to Verify?

Moderator: Sandeep Shukla—Virginia Tech, U.S.A.

Panelists: John Sanguinetti—Forte Design Systems; Brian Bailey—Industry Verification Guru; Andres Takach—Mentor Graphics; Chad Spackmana—Cebatech; Ajit Dingankar—Intel; Hiren Patel—University of Waterloo, Canada

Abstract: The panelists will debate whether SystemC is going to become a de facto design language or will it remain a verification and performance modeling language. It will result in an inspiring debate on the recent trends from the makers of SystemC based synthesis tools, users of SystemC for design and verification, and academic researchers.
Session 6: Test and Debug

Fault Table Generation Using Graphics Processing Units ................................................................. 60
  Kanupriya Gulati and Sunil P. Khatri—Texas A&M University, U.S.A.

Diagnostic Test Generation for Silicon Diagnosis with an Incremental Learning Framework Based on
Search State Compatibility ............................................................................................................. 68
  Maheshwar Chandrasekar and Michael S. Hsiao—Virginia Tech, U.S.A.

TG-Pro: A New Model for SAT-Based ATPG .................................................................................... 76
  Huan Chen and Joao Marques-Silva—University College Dublin, Ireland

Localizing Transient Faults Using Dynamic Bayesian Networks ................................................ 82
  Susmit Jha, Wenchao Li and Sanjit A. Seshia—University of California, Berkeley, U.S.A.

Session 7: Invited Session—High-Level Modeling and Validation

An Instrumented Observability Coverage Method for System Validation ...................................... 88
  Peter Lisherness and Kwang-Ting (Tim) Cheng—University of California, Santa Barbara, U.S.A.

A Symbolic Execution Framework for Algorithm-Level Modelling ............................................. 94
  Ziyad Hanna and Tom Melham—University of Oxford, U.K.

Dynamic Verification of Multicore Communication Applications in MCAPI ............................. 100
  Subodh Sharma and Ganesh Gopalakrishnan—University of Utah, U.S.A.;
  Eric Mercer—Brigham Young University, U.S.A.

Session 8: System Validation Approaches

Airwolf-TG: A Test Generator for Assertion-Based Dynamic Verification .................................. 106
  Jason G. Tong, Marc Boulé and Zeljko Zilic—McGill University, Canada

A Versatile Scheme for the Validation, Testing and Debugging of High Speed Serial Interfaces 114
  Yongquan Fan and Zeljko Zilic—McGill University, Canada

Experience with Widening based Equivalence Checking in Realistic Multimedia Systems .......... 122
  Sven Verdoolaege—Katholieke Universiteit Leuven, Belgium; Martin Palkovic—IMEC, Belgium;
  Maurice Bruynooghe and Gerda Janssens—Katholieke Universiteit Leuven, Belgium;
  Francky Catthoor—IMEC and Katholieke Universiteit Leuven, Belgium

Session 9: Improved Verification Techniques

A Coordinated Reachability Analysis Method for Modular Verification of Asynchronous Designs 130
  Hao Zheng—University of South Florida, U.S.A.

Modular Arithmetic Decision Procedure with Auto-Correction Mechanism ............................. 138
  Bijan Alizadeh and Masahiro Fujita—University of Tokyo and CREST, Japan

Activity-based Refinement for Abstraction-Guided Simulation ................................................ 146
  Debapriya Chatterjee and Valeria Bertacco—University of Michigan, U.S.A.
Session 10: Invited Session—Post-Silicon Validation and Debug

IFRA: Post-Silicon Bug Localization in Processors ................................................................. 154
Sung-Boem Park and Subhasish Mitra—Stanford University, U.S.A.

RTL DFT Techniques to Enhance Defect Coverage for Functional Test Sequences .......................... 160
Hongxia Fang and Krishnendu Chakrabarty—Duke University, U.S.A.;
Hideo Fujiwara—Nara Institute of Science and Technology, Japan

Hardware Trojan: Threats and Emerging Solutions .................................................................. 166
Rajat Subhra Chakraborty, Seetharam Narasimhan and
Swarup Bhunia—Case Western Reserve University, U.S.A.

Design-for-Debug for Post-Silicon Validation: Can High-Level Descriptions Help? .................. 172
Nicola Nicolici and Ho Fai Ko—McMaster University, Canada

Author Index