2010 IEEE/ACM/IFIP
International Conference on
Hardware/Software Codesign and
System Synthesis

(CODES+ISSS 2010)

Scottsdale, Arizona, USA
24 – 29 October 2010
Keynote Talk
Session Chair: Karam Chatha (Arizona State University)
Embedded Market: Challenges and Opportunities (Page 1)
Vida Ilderem (Intel Corporation)

Session 1A: Application-Specific Algorithms and Architectures
Session Chairs: Robert A. Walker (Kent University)
Todor Stefanov (LIACS)

Best Paper Nominee
Rank Based Dynamic Voltage and Frequency Scaling for Tiled Graphics Processors (Page 3)
B.V.N. Silpa (Indian Institute of Technology Delhi)
Gummidi P. Krishnaiah (Indian Institute of Technology Delhi)
Preeti Ranjan Panda (Indian Institute of Technology Delhi)

Intermediate Fabrics: Virtual Architectures for Circuit Portability and Fast Placement and Routing (Page 13)
James Coole (University of Florida)
Greg Stitt (University of Florida)

An Elastic Software Cache with Fast Prefetching for Motion Compensation in Video Decoding (Page 23)
Ping Chao (National Tsing Hua University)
Youn-Long Lin (National Tsing Hua University)

Session 1B: Reconfigurable and Real-time System
Session Chairs: Sudarshan Banerjee (UCI)
Pai Chou (UCI)

Verification of Dynamically Reconfigurable Embedded Systems by Model Transformation Rules (Page 33)
Felix Madlener (Technische Universität Darmstadt)
Julia Weingart (Technische Universität Darmstadt)
Sorin A. Huss (Technische Universität Darmstadt)

Hardware/Software Optimization of Error Detection Implementation for Real-Time Embedded Systems (Page 41)
Adrian Lifa (Linköping University)
Petru Eles (Linköping University)
Zebo Peng (Linköping University)
Viacheslav Izosimov (Embedded Intelligent Solutions)

Scheduling Garbage Collection in Real-Time Systems (Page 51)
Martin Kero (Luleå University of Technology)
Simon Aittamaa (Luleå University of Technology)

Session 2A: Special Session - From ESL-2010 to ESL-2015
Session Chairs: Adam Donlin (Xilinx)
Karam Chatha (Arizona State University)

From ESL 2010 to ESL 2015 (Page 61)
Tor Jeremiasen (Texas Instruments)
Tim Kogel (Synopsys)
Andres Takach (Mentor Graphics)
Grant Martin (Tensilica)
Adam Donlin (Xilinx)
Karam Chatha (Arizona State University)

Session 2B: Special Session - HW/SW Co-design for High Performance Computing: Challenges and Opportunities
Session Chairs: X. Sharon Hu (Notre Dame)
Richard Murphy (Sandia National Laboratories)
Hardware/Software Co-Design for High Performance Computing: Challenges and Opportunities
X. Sharon Hu (University of Notre Dame)
Richard C. Murphy (Sandia National Laboratories)
Sudip Dosanjh (Sandia National Laboratories)
Kunle Olukotun (Stanford University)
Stephen Poole (Oak Ridge National Laboratory)

Session 3A: Optimising Multiprocessor and NoC Platforms for Performance, QoS, and Reliability
Session Chairs: Rainer Doemer (UCI)
Frank Vahid (UCR)

Best Paper Nominee
Exploring Programming Model-Driven QoS Support for NoC-Based Platforms
Jaume Joven (Ecole Polytechnic Federale Lausanne)
Andrea Marongiu (University of Bologna)
Federico Angiolini (iNoCs SarL)
Luca Benini (University of Bologna)
Giovanni De Micheli (LSI-EPFL)

Optimal Synthesis of Latency and Throughput Constrained Pipelined MPSoCs Targeting Streaming Applications
Haris Javaid (University of New South Wales)
Xin He (University of New South Wales)
Aleksandar Ignjatovic (University of New South Wales)
Sri Parameswaran (University of New South Wales)

OEtIE: A Novel Turn Model Based Fault Tolerant Routing Scheme for Networks-on-Chip
Sudeep Pasricha (Colorado State University)
Yong Zou (Colorado State University)
Dan Connors (University of Colorado Denver)
Howard Jay Siegel (Colorado State University)

Session 3B: Power-Aware Design
Session Chairs: Sarma Vrudhula (Arizona State University)
Naehyuck Chang (SNU)

Power Aware SID-Based Simulator for Embedded Multicore DSP Subsystems
Cheng-Yen Lin (National Tsing-Hua University)
Po-Yu Chen (National Tsing-Hua University)
Chun-Kai Tseng (National Tsing-Hua University)
Chang-Wen Huang (National Tsing-Hua University)
Chia-Chieh Weng (National Tsing-Hua University)
Chi-Bang Kuan (National Tsing-Hua University)
Shih-Han Lin (National Tsing-Hua University)
Shi-Yu Huang (National Tsing-Hua University)
Jenq-Kuen Lee (National Tsing-Hua University)

Accurate Online Power Estimation and Automatic Battery Behavior Based Power Model Generation for Smartphones
Lide Zhang (University of Michigan)
Birjodh Tiwana (University of Michigan)
Zhiyuan Qian (University of Michigan)
Zhaoguang Wang (University of Michigan)
Robert P. Dick (University of Michigan)
Zhuoqing Morley Mao (University of Michigan)
Lei Yang (Google Inc)

Statistical Approach in a System Level Methodology to Deal with Process Variation
Concepción Sanz Pineda (Universidad Complutense de Madrid)
Manuel Prieto (Universidad Complutense de Madrid)
José Ignacio Gómez (Universidad Complutense de Madrid)
Christian Tezliado (Universidad Complutense de Madrid)
Francky Catthoor (Inter-University Microelectronics Center - IMEC)

Session 4A: MPSoC: Analysis and Synthesis
Session Chairs: Andreas Gerstlauer (University of Texas)
Roman Lysecky (University of Arizona)

Best Paper Nominee
Worst-Case Performance Analysis of Synchronous Dataflow Scenarios
Marc Geilen (Eindhoven University of Technology)
Sander Stuijk (Eindhoven University of Technology)

Improving Platform-Based System Synthesis by Satisfiability Modulo Theories Solving
Felix Reimann (University of Erlangen-Nuremberg)
Michael Gläβ (University of Erlangen-Nuremberg)
Christian Haubelt (University of Erlangen-Nuremberg)
Michael Eberl (University of Erlangen-Nuremberg)
Jürgen Teich (University of Erlangen-Nuremberg)
A Case for Lifetime-Aware Task Mapping in Embedded Chip Multiprocessors
Adam S. Hartman (Carnegie Mellon University)
Donald E. Thomas (Carnegie Mellon University)
Brett H. Meyer (University of Virginia)

Session 4B: Memory and Communication Architecture
Session Chairs: Sudeep Pasricha (Colorado State University)
Christian Haubelt (FAU)

Automatic Memory Partitioning: Increasing Memory Parallelism via Data Structure Partitioning
Yosi Ben Asher (Haida University)
Nadav Rotem (Haifa University)

Towards a Synthesis Semantics for SystemC Channels
Kim Grüttner (OFFIS - Institute for Information Technology, Germany)
Hannan Kli (OFFIS - Institute for Information Technology, Germany)
Frank Oppenheimer (OFFIS - Institute for Information Technology, Germany)
Achim Renkberg (Carl von Ossietzky University Oldenburg)
Wolfgang Nebel (Carl von Ossietzky University Oldenburg)

Demand-Based Block-Level Address Mapping in Large-Scale NAND Flash Storage Systems
Zhiwei Qin (The Hong Kong Polytechnic University)
Yi Wang (The Hong Kong Polytechnic University)
Duo Liu (The Hong Kong Polytechnic University)
Zili Shao (The Hong Kong Polytechnic University)

Session 5A: Embedded Tutorial — An Introduction to the SystemC Synthesis Subset Standard
Session Chair: Andres Takach (Mentor Graphics)

An Introduction to the SystemC Synthesis Subset Standard
Philippe Cousseau (Université de Bretagne-Sud)
Andres Takach (Mentor Graphics)
Michael McNamara (Cadence)
Mike Meredith (Forte Design Systems)

Session 5B: Embedded Tutorial - Compilation Techniques for CGRAs: Exploring all Parallelization Approaches
Session Chair: Tom Vander Aa (IMEC, Belgium)

Compilation Techniques for CGRAs: Exploring All Parallelization Approaches
Tom Vander Aa (IMEC, Belgium)
Praveen Raghavan (IMEC, Belgium)
Scott Mahlke (University of Michigan)
Bjorn De Sutter (Ghent University)
Aviral Shrivastava (Arizona State University)
Frank Hannig (University of Erlangen-Nuremberg)

Session 6A: Memory Architecture for Embedded Systems
Session Chairs: Joerg Henkel (Karlsruhe Institute of Technology)
Andy Pimentel (University of Amsterdam)

Dynamic, Non-Linear Cache Architecture for Power-Sensitive Mobile Processors
Garo Bournoutian (University of California, San Diego)
Alex Orailoglu (University of California, San Diego)

A Greedy Buffer Allocation Algorithm for Power-Aware Communication in Body Sensor Networks
Hassan Ghaseemazdeh (University of Texas at Dallas)
Roozbeh Jafari (University of Texas at Dallas)

High Durability in NAND Flash Memory Through Effective Page Reuse Mechanisms
Kwangyoon Lee (University of California, San Diego)
Alex Orailoglu (University of California, San Diego)

Session 6B: New Design Approaches for Network-on-Chip Systems
Session Chairs: Sudeep Pasricha (Colorado State University)
Kees Goossens (TUE)

A Holistic Approach to Network-on-Chip Synthesis
Glenn Leary (Arizona State University)
Karam S. Chatha (Arizona State University)

NeuroNoC: Neural Network Inspired Runtime Adaptation for an On-chip Communication Architecture
Thomas Ebi (Karlsruhe Institute of Technology)
Mohammad Abdullah Al Faruque (Karlsruhe Institute of Technology)
Jörg Henkel (Karlsruhe Institute of Technology)

Workload Characterization and Its Impact on Multicore Platform Design
Paul Bogdan (Carnegie Mellon University)
Radu Marculescu (Carnegie Mellon University)

Session 7A: Novel Techniques for Accelerating System Simulation
Session Chairs: Tim Koegel (Synopsys)
Rainer Doemer (UCI)

parSC: Synchronous Parallel SystemC Simulation on Multi-Core Host Architectures (Page 241)
Christoph Schumacher (RWTH Aachen University)
Rainer Leupers (RWTH Aachen University)
Dietmar Petras (Synopsys, Inc.)
Andreas Hoffmann (Synopsys, Inc.)

FastFwd: An Efficient Hardware Acceleration Technique for Trace-Driven Network-on-Chip Simulation (Page 247)
Gummidipudi Krishnaiah (IIT Delhi)
B.V.N. Silpa (IIT Delhi)
Preeti Ranjan Panda (IIT Delhi)
Anshul Kumar (IIT Delhi)

Session 7B: Embedded Software Performance Optimization
Session Chairs: Aviral Shrivastava (Arizona State University)
Preeti Ranjan Panda (IITD)

Automatic Parallelization of Embedded Software Using Hierarchical Task Graphs and Integer Linear Programming (Page 267)
Daniel Cordes (Informatik Centrum Dortmund e.V.)
Peter Marwedel (Informatik Centrum Dortmund e.V.)
Arindam Mallik (Imec Belgium)

Performance Modeling of Embedded Applications with Zero Architectural Knowledge (Page 277)
Marco Lattuada (Politecnico di Milano)
Fabrizio Ferrandi (Politecnico di Milano)

A Performance Model and Code Overlay Generator for Scratchpad Enhanced Embedded Processors (Page 287)
Michael A. Baker (Arizona State University & U.S. Army Research Laboratory)
Amrit Panda (Arizona State University)
Nikhil Ghadge (Arizona State University)
Aniruddha Kadne (Arizona State University)
Karan S. Chatha (Arizona State University)

Session 8A: Reliability and Memory Issues in MPSoCs
Session Chairs: Aseem Gupta (Freescale)
Paul Pop (TU Denmark)

System-Level Reliability Modeling for MPSoCs (Page 297)
Yun Xiang (University of Michigan)
Thidapat Chantem (University of Notre Dame)
Robert P. Dick (University of Michigan)
X. Sharon Hu (University of Notre Dame)
Li Shang (University of Colorado)

A Task Remapping Technique for Reliable Multi-Core Embedded Systems (Page 307)
Chanhee Lee (Seoul National University)
Hokeun Kim (Seoul National University)
Hae-woo Park (Seoul National University)
Sungchan Kim (Chonbuk National University)
Hyunok Oh (Hanyang University)
Soonhoi Ha (Seoul National University)

Heap Data Management for Limited Local Memory (LLM) Multi-Core Processors (Page 317)
Ke Bai (Arizona State University)
Aviral Shrivastava (Arizona State University)

Session 8B: Special Session - Unconventional Fabrics, Architectures, and Models for Future Multi-core Systems
Session Chair: Radu Marculescu (Carnegie Mellon University)

Unconventional Fabrics, Architectures, and Models for Future Multi-Core Systems (Page 327)
Radu Marculescu (Carnegie Mellon University)
Christof Teuscher (Portland State University)
Partha Pratim Pande (Washington State University)

Tutorials

Modeling and Analyzing Real-Time Multiprocessor Systems (Page 329)
Maarten Wiggers (University of Twente)
Lothar Thiele (ETH Zurich)
Edward A. Lee (University of California, Berkeley)
Simon Schleiereck (Technische Universität Braunschweig)
Marco Bekooij (NXP Semiconductors)

Exploring Models of Computation with Ptolemy II (Page 331)
Christopher X. Brooks (University of California, Berkeley)
Edward A. Lee (University of California, Berkeley)
Stavros Tripakis (University of California, Berkeley)