Table of Contents

*Tutorials.*

Dimensions in Program Synthesis ................................................................. 1  
*Sumit Gulwani*

Verifying VIA Nano Microprocessor Components ........................................ 3  
*Warren A. Hunt, Jr.*

**Session 1. Invited Talk**

Embedded Systems Design: Scientific Challenges and Work Directions .......... 11  
*Joseph Sifakis*

**Session 2. Industrial Track – Case Studies**

Formal Verification of an ASIC Ethernet Switch Block ............................... 13  
*Balekudru Krishna, Anamaya Sullerey, Alok Jain*

Formal Verification of Arbiters using Property Strengthening and  
Under-approximations .................................................................................. 21  
*Gadiel Auerbach, Fady Copty, Viresh Paruthi*

SAT-Based Semiformal Verification of Hardware........................................... 25  
*Sabih Agbaria, Dan Carmi, Orly Cohen, Dmitry Korchemny, Michael Lifshits,  
Alexander Nadel*

DFT Logic Verification through Property Based Formal Methods -  
SOC to IP ...................................................................................................... 33  
*Lopamudra Sen, Supriya Bhattacharjee, Amit Roy, Bijitendra Mittra, Subir K Roy*

**Session 3. Software Verification**

SLAM2: Static Driver Verification with Under 4% False Alarms .................... 35  
*Thomas Ball, Ella Bounimova, Rahul Kumar, Vladimir Levin*
Precise Static Analysis of Untrusted Driver Binaries ............................................. 43
Johannes Kinder, Helmut Veith

Verifying SystemC: a Software Model Checking Approach ......................... 51
Alessandro Cimatti, Andrea Micheli, Iman Narasamdy, Marco Roveri

Session 4. Decision Procedures

Coping with Moore's Law (and More): Supporting Arrays in State-of-the-Art
Model Checkers ........................................................................................................ 61
Jason Baumgartner, Michael Case, Hari Mony

CalCS: SMT Solving for Nonlinear Convex Constraints ............................ 71
Pierluigi Nuzzo, Alberto Puggelli, Sanjit Seshia, Alberto Sangiovanni-Vincentelli

Integrating ICP and LRA Solvers for Deciding Nonlinear Real Arithmetic
Problems .................................................................................................................. 81
Sicun Gao, Malay Ganai, Franjo Ivancic, Aarti Gupta, Sriram Sankaranarayanan,
Edmund Clarke

Session 5. Synthesis

A Halting Algorithm to Determine the Existence of Decoder ....................... 91
ShengYu Shen, Ying Qin, Jianmin Zhang, SiKun Li

Synthesis for Regular Specifications over Unbounded Domains ................. 101
Jad Hamza, Barbara Jobstmann, Viktor Kuncak

Automatic Inference of Memory Fences ......................................................... 111
Michael Kuperstein, Martin Vechev, Eran Yahav

Session 6. Industrial Track

Applying SMT in Symbolic Execution of Microcode ................................. 121
Anders Franzen, Alessandro Cimatti, Alexander Nadel, Roberto Sebastiani,
Jonathan Shalev

Automated Formal Verification of Processors Based on Architectural Models . 129
Ulrich Kuehne, Sven Beyer, Joerg Bormann, John Barstow
Encoding Industrial Hardware Verification Problems into Effectively Propositional Logic

Zurab Khasidashvili, Moshe Emmer, Konstantin Korovin, Andrei Voronkov

Session 7. Hardware and Protocol Verification

Combinational Techniques for Sequential Equivalence Checking

Hamid Savoj, David Berthelot, Alan Mishchenko, Robert Brayton

Automatic Verification of Estimate Functions with Polynomials of Bounded Functions

Jun Sawada

A Framework for Incremental Modelling and Verification of On-Chip Protocols

Peter Boehm

Modular Specification and Verification of Interprocess Communication

Eyad Alkassar, Ernie Cohen, Mark Hillebrand, Hristo Pentchev

Session 8. Invited Talk

Large-scale Formal Application: From Fiction to Fact

Viresh Paruthi

Session 9. Abstraction

A Single-Instance Incremental SAT Formulation of Proof-and Counterexample-Based Abstraction

Niklas Een, Alan Mishchenko, Nina Amla

Predicate Abstraction with Adjustable-Block Encoding

Dirk Beyer, M. Erkan Keremoglu, Philipp Wendler

Modular Bug Detection with Inertial Refinement

Nishant Sinha
Path Predicate Abstraction by Complete Interval Property Checking ............... 207
Joakim Urdahl, Dominik Stoffel, Jörg Bormann, Markus Wedler, Wolfgang Kunz

Session 10. SAT and QBF

Relieving Capacity Limits on FPGA-based SAT-solvers ................................. 217
Leopold Haller, Satnam Singh

Boosting Minimal Unsatisfiable Core Extraction ................................. 221
Alexander Nadel

Propelling SAT and SAT-based BMC using Careset ................................. 231
Malay Ganai

Efficiently Solving Quantified Bit-Vector Formulas ................................. 239
Christoph Wintersteiger, Youssef Hamadi, Leonardo de Moura

Session 11. Verification of Concurrent Systems

Boosting Multi-Core Reachability Performance with Shared Hash Tables ...... 247
Alfons Laarman, Jaco van de Pol, Michael Weber

Incremental Component-based Construction and Verification using Invariants ................................. 257
Saddek Bensalem, Marius Bozga, Axel Legay, Thanh-Hung Nguyen, Joseph Sifakis, Rongjie Yan

Verifying Shadow Page Table Algorithms ................................................. 267
Eyad Alkassar, Ernie Cohen, Mark Hillebrand, Mikhail Kovalev, Wolfgang Paul

Exhibition.

Impacting Verification Closure using Formal Analysis (abstract) ................. 271
Massimo Roselli

Scalable and Precise Program Analysis at NEC (abstract) ......................... 273
Gogul Balakrishnan, Malay Ganai, Aarti Gupta, Franjo Ivancic, Vineet Kahlon, Weihong Li, Naoto Maeda, Nadia Papakonstantinou, Sriram Sankaranarayanan, Nishant Sinha, Chao Wang
Achieving Earlier Verification Closure Using Advanced Formal Verification
(abstract) ...................................................................................................................... 275
Michael Siegel

PINCETTE - Validating Changes and Upgrades in Networked Software (abstract) .......................................................... 277
Hana Chockler