2011 IEEE International Conference on IC Design & Technology

(ICICDT 2011)

Kaohsiung, Taiwan
2-4 May 2011
Session A: I/O Circuits and ESD Protection

**Transient-to-Digital Converter to Detect Electrical Fast Transient (EFT) Disturbance for System Protection Design 001**

Cheng-Cheng Yen¹, Wan-Yen Lin¹, Ming-Dou Ker¹,², Ching-Ling Tsai³, Shih-Fan Chen³, Tung-Yang Chen³

¹Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan
²Department of Electronics Engineering, I-Shou University, Kaohsiung, Taiwan
³Himax Technologies Inc., Taiwan

**ESD RF Protections in Advanced CMOS Technologies and its Parasitic Capacitance Evaluation 005**

Ph. Galy¹, J. Jimenez¹, P. Meuris², W. Schoenmaker², O. Dupuis²

¹STMicroelectronics, Crolles, France
²MAGWEL NV, Leuven, Belgium

**Design of Low-Leakage Power-Rail ESD Clamp Circuit with MOM Capacitor and STSCR in a 65-nm CMOS Process 009**

Po-Yen Chiu¹, Ming-Dou Ker¹,²

¹Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan
²Dept. of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan

Session B: Advanced Transistor/Material

**Invited Paper: Low power UTBOX and Back Plane (BP) FDSOI technology for 32nm node and below 013**

C. Fenouillet-Beranger¹,², P. Perreau¹,², L. Tosti², O. Thomas², J-P. Noel¹, O. Weber², F. Andrieu², A. Bajolet¹, S. Haendler¹, F. Boedt¹, O. Faynot², F. Boeuf²

¹STMicroelectronics, Crolles, France
²CEA/LETI-Minatec, Grenoble, France
³SOITEC, Parc Technologique des Fontaines, Bernin, France

**Electrical Characteristic Fluctuation of 16 nm MOSFETs Induced by Random Dopants and Interface Traps 017**

Yung-Yueh Chiu¹, Fu-Hai Li¹, Hui-Wen Cheng¹, Yiming Li²

¹Institute of Communications Engineering, National Chiao-Tung University, Hsinchu, Taiwan.
²Department of Electrical Engineering and Institute of Communications Engineering, National Chiao-Tung University, Hsinchu, Taiwan

**Invited Paper: Excellent Silicon Thickness Uniformity on Ultra-Thin SOI for controlling Vt variation of FDSOI 021**

W. Schwarzenbach, X. Cauchy, F. Boedt, O. Bonnin, E. Butaud, C. Girard, B.-Y. Nguyen, C. Mazure, C. Maleville

SOITEC, Parc Technologique des Fontaines – Bernin – Crolles – France

**Variability Analysis of UTB SOI Subthreshold SRAM Considering Line-Edge Roughness, Work Function Variation and Temperature Sensitivity 024**

Vita Pi-Ho Hu, Ming-Long Fan, Pin Su, Ching-Te Chuang

Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan

**Invited Paper: 3D Integrable Nanowire FET Sensor with Intrinsic Sensitivity Boost 028**

Chi On Chui, Jorge Kina, Kyeong-Sik Shin

Department of Electrical Engineering, University of California, Los Angeles, CA, USA

**On The Magnitude of Random Telegraph Noise in Ultra-Scaled MOSFETs 032**

K.P. Cheung, J.P. Campbell

Semiconductor Electronics Division, NIST, Gaithersburg, MD, USA
Session C: DFM/DFT/DFR/DFY

Invited Paper: Timing Error Prevention using Elastic Clocking 036
Kwanyeob Chae, Chang-Ho Lee, Saibal Mukhopadhyay
Georgia Institute of Technology, Atlanta, GA, USA

Time and Workload Dependent Device Variability in Circuit Simulations 040
D. Rodopoulos, S. Mahato, V. Valduga de Almeida Camargo, B. Kaczer, F. Catthoor, S. Cosemans, G. Groeseneken, A. Papanicolaou, D. Soudris
IMEC, Leuven, Belgium

Kumpei Yoshikawa¹, Takushi Hashida¹, Makoto Nagata¹,²
¹Graduate School of System Informatics, Kobe University, Nada-ku, Kobe, Japan
²CREST, JST, Japan

Interconnect Test for Core-based Designs with Known Circuit Characteristics and Test Patterns 049
Tung-Hua Yeh¹, Sying-Jyan Wang¹, Katherine Shu-Min Li¹
¹Department of Computer Science and Engineering, National Chung-Hsing University Taichung, Taiwan
²Department of Computer Science and Engineering, National Sun-Yat Sen University Kaohsiung, Taiwan

Invited Paper: Architectural-Level Error-Tolerant Techniques for Low Supply Voltage Cache Operation 053
Shih-Lien Lu, Alaa Alameeldeen, Keith Bowman, Zeshan Chishti, Chris Wilkerson, Wei Wu
Intel Labs, Hillsboro Oregon, USA

Session D: 3D Integration

Invited Paper: Special Considerations for 3DIC Circuit Design and Modeling 058
Sally Liu, Yung-Chow Peng, Fu-Lung Hsueh
Taiwan Semiconductor Manufacturing Company, Hsinchu Science Park, Hsinchu, Taiwan, ROC

A Single TSV-rail 3D Quasi Delay Insensitive Asynchronous Signaling 061
M. Belleville, E. Beigne, A. Valentian
CEA, LETI, MINATEC Campus, Grenoble, France

Invited Paper: Smart Stacking™ Technology: an Industrial Solution for 3D Layer Stacking 065
C. Lagahe Blanchard¹, I. Radu¹, M. Sadaka², K. Landry³
¹SOITEC, Parc Technologique des Fontaines, Bernin, Crolles Cedex, France
²SOITEC USA Inc., Austin, Texas, USA

TSV Number Minimization Using Alternative Paths 068
Chun-Hua Cheng, Chih-Hsien Kuo, Shih-Hsu Huanga
Department of Electronic Engineering, Chung Yuan Christian University, Chung Li, Taiwan, R.O.C.

Invited Paper: Through Silicon Via Technology using Tungsten Metallization 072
G. Parès¹, N. Bresson², S. Minoret¹, V. Lapras¹, P. Brianceau¹, J.F. Lugand¹, R. Anciant¹, N. Sillon¹
¹CEA/LETI – Minatec, France
²SOITEC France

Session E: CAD

Statistical Delay Calculation with Multiple Input Simultaneous Switching 077
Qin Tang, Amir Zjajo, Michel Berkelaar and Nick van der Meij
Circuits and Systems Group, Delft University of Technology, The Netherlands
Balanced Truncation of a Stable Non-Minimal Deep-Submicron CMOS Interconnect 081
Amir Zjajo, Qin Tang, Michel Berkelaar, Nick van der Meij
Circuits and Systems Group, Delft University of Technology, The Netherlands

Enabling TLM-2.0 Interface on QEMU and SystemC-based VirtualPlatform 085
Tse-Chen Yeh, Zin-Yuan Lin, Ming-Chao Chiang
Department of Computer Science and Engineering, National Sun Yat-sen University, Kaohsiung, Taiwan

A Fast Custom Network Topology Generation with Floorplanning for NoC-based Systems 089
Katherine Shu-Min Li, Shu-Yu Chen, Liang-Bi Chen, Ruei-Ting Gu
Department of Computer Science and Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan

Session F: Advanced Memory Device

Invited Paper: Evolution of Embedded Flash Memory Technology for MCU 093
Hideto Hidaka
Renesas Electronics Corp. Itami, Hyogo, Japan

Impacts of Intrinsic Device Variations on the Stability of FinFET Subthreshold SRAMs 097
Yin-Nien Chen, Chien-Yu Hsieh, Ming-Long Fan, Vita Pi-Ho Hu, Pin Su and Ching-Te Chuang
Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan

Invited Paper: Low-Cost Embedded Flash Memory Technology 101
Wein-Town Sun1, Cheng-Jye Liu1, Chun-Yuan Lo1, Yun-Jen Ting1, Ying-Je Chen1, Tai-Yi Wu1, Eng-Huat Toh2, Xiao-Hong Yuan2, Ko-Li Low2, Qiu Han2, Young-Seon You2, Ying-Keung Leung2, Swee-Tuck Woo2
1eMemory Technology Inc., Hsinchu County, Taiwan
2GLOBALFOUNDRIES Singapore Pte. Ltd., Singapore

Session G: Reliability/Plasma Induced Damage

Invited Paper: Crystallization Technique of Epitaxial HfO2 Thin Films on Si Substrates and their Potential for Advanced High-k Gate Stack Technology 106
Shinji Migita, Hiroyuki Ota
Nanodevice Innovation Research Center, National Institute of Advanced Industrial Science and Technology, Tsukuba, Ibaraki, Japan

A New Prediction Model for Effects of Plasma-Induced Damage on Parameter Variations in Advanced LSIs 110
Koji Eriguchi, Yoshinori Takao, Kouichi Ono
Kyoto University, Yoshida-Honmachi, Sakyo-ku, Kyoto, Japan

Invited Paper: Impact of La on the Bias-Temperature Instability of the HfSiO High-κ N-MOSFET 114
D. S. Ang1, G. A. Du2
1School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore
2GLOBALFOUNDRIES Singapore Pte. Ltd., Singapore

Separation of NBTI Component from Channel Hot Carrier Degradation in pMOSFETs Focusing on Recovery Phenomenon 118
Y. Mitani1, S. Fukatsu2, D. Hagishima3, K. Matsuzawa1
1Advanced LSI Technology Laboratory, Corporate R&D Center, Toshiba Corporation, Yokohama, Japan
2Device Process Development Center, Toshiba Corporation, Japan
3Toshiba Semiconductor Company, Japan
Session H: High Power/High Voltage

On the Impact of the Edge Profile of Interconnects on the Occurrence of Passivation Cracks of Plastic-Encapsulated Electronic Power Devices 122
Jan Ackaert1, Daniel Vanderstraeten1, Bart Vandevelde2
1Corporate R&D, ON Semiconductors, Oudenaarde, Belgium
2imec, Leuven, Belgium

Domestic Indirect Feedback Compensation of Multiple-Stage Amplifiers for Multiple-Voltage Level-Converting Amplification 126
Shang-Hsien Yang, Chua-Chin Wang
Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan

Session I: Low Power

Microwatt Low-noise Variable-Gain Amplifier 130
Chun-Yi Li, Yu-Bin Lin, Robert Rieger
Electrical Engineering Department, National Sun Yat-Sen University, Kaohsiung, Taiwan

Invited Paper: SRAM Bitcell Design for Low Voltage Operation in Deep Submicron Technologies 134
Young Hwi Yang1, Jisu Kim1, Hyunkook Park1, Joseph Wang2, Geoffrey Yeap2, Seong-Ook Jung3
1School of Electrical and Electronic Engineering, Yonsei University, Seoul, Korea
2Qualcomm Inc., San Diego, CA, USA.

Ming-Hsien Tsai1,2, Shawn S. H. Hsu1, Fu-Lung Hsueh1, Chewn-Pu Jou2, Tzu-Jin Yeh2, Ming-Hsiang Song2, Jen-Chou Tseng2
1Dept. of Electrical Engineering and Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan
2Design Technology Division, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan

Invited Paper: Low Power Embedded Memory Design – Process to System Level Considerations 142
Esin Terzioglu, Sei Seung Yoon, ChangHo Jung, Ritu Chaba, Venu Boynapalli, Mohamed Abu-Rahma, Joseph Wang, Sam Yang, Giri Nallapati, Aaron Thean, Chidi Chidambaran, Michael Han, Geoffrey Yeap, Mehdi Sani
Qualcomm Inc., San Diego, CA, USA

65nm PD-SOI Glitch-Free Retention Flip-Flop for MTCMOS Power Switch applications 147
J. Le-Coz1, P. Flatresse1, S. Clerc1, M.Belleville2, A. Valentian2
1STMicroelectronics, Crolles, France
2CEA LETI, MINATEC campus, Grenoble, France

Session J: RF & Analog, Mixed signal

An Ultra-Low Energy Capacitive DAC Array switching Scheme for SAR ADC in Biomedical Applications 151
Chao Yuan, Yvonne Y. H. Lam
School of Electrical and Electronics Engineering, VIRTUS, IC Design Centre of Excellence, Nanyang Technological University, Singapore

Slew-Rate Controlled Output Stages for Switching DC-DC Converters 155
Jia-Ming Liu, Yi-Cheng Huang, Yu-Chun Ying, Tai-Haur Kuo
Department of Electrical Engineering, National Cheng Kung University, Tainan City, Taiwan
Temperature Dependence of Device Mismatch and Harmonic Distortion in Nanoscale Uniaxial-Strained PMOSFETs 159
Jack J.-Y. Kuo, William P.-N. Chen, Pin Su
Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan

A 8-bit 50-Msamples/s Switched-Current Pipelined ADC with Residue Generator and Interlaced Stage 163
Guo-Ming Sung, Ying-Tzu Lai
Department of Electrical Engineering, National Taipei University of Technology, Taipei, Taiwan

Continuously Auto-Tuned and Self-Ranged Dual-Path PLL Design with Hybrid AFC 167
Min Wang, Bo Zhou, Woogeun Rhee, Zhihua Wang
Institute of Microelectronics, Tsinghua University, Beijing, China

Session K: SoC/MPSoC/SIP

An Integrated HDTV Predictive Pixel Compensator for H.264/AVC Decoder 171
Ting-Chi Tong, Yun-Nan Chang
Department of Computer Science and Engineering, National Sun Yat-sen University, Kaohsiung, Taiwan

Invited Paper: IBM zEnterprise™ Energy Efficient 5.2Ghz Processor Chip 175
1IBM Systems and Technology Group, Austin, TX, USA
2IBM Systems and Technology Group, Yorktown Heights, NY, USA
3IBM Systems and Technology Group, Poughkeepsie, NY, USA
4IBM Systems and Technology Group, Boeblingen, Germany

Ultra-Low Power FIR Filter using STSC-CVL Logic 180
Sajib Roy, Md. Murad Kabir Nipun, J Jacob Wikner
Division of Electronic Systems, Linkoping University, Sweden

Design of a Low-Cost Floating-Point Programmable Vertex Processor for Mobile Graphics Applications Based on Hybrid Number System 184
Shen-Fu Hsiao, Chan-Feng Chiu, Chia-Sheng Wen
Department of Computer Science and Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan

Session L: I/O Circuits and ESD Protection

A Low Jitter Active Body-Biasing Control-based Output Buffer in 65nm PD-SOI 188
Dimitri Soussan1,2, Sylvain Majcherczak1, Alexandre Valentian2, Marc Belleville2
1STMicroelectronics Crolles, Crolles, France
2CEA LETI, Minatec campus, Grenoble, France

Adaptable Stimulus Driver for Epileptic Seizure Suppression 192
Ming-Dou Ker1,2, Wei-Ling Chen1, Chun-Yu Lin1
1Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan
2Department of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan

Gate-Driven 3.3V ESD Clamp Using 1.8V Transistors 196
Guang-Cheng Wang, Chia-Hui Chen, Wen-Hsin Huang, Kuo-Ji Chen, Ming-Hsiang Song, Ta-Pen Guo
Taiwan Semiconductor Manufacturing Corp., Hsinchu, Taiwan

Beta-Matrix ESD Network: throughout End of Placement Rules? 199
J. Bourgeat, P. Galy, B. Jacquier
STMicroelectronics, Crolles, France
Invited Paper: Design of on-chip Transient Voltage Suppressor in a Silicon-based Transceiver IC to meet IEC System-Level ESD Specification
Ryan Hsin-Chin Jiang, Tang-Kuei Tseng, Chi-Hao Chen, Che-Hao Chuang
Amazing Microelectronic Corp., HsinChiu, Taiwan R.O.C.

Session M: Soft Error Rate

Invited Paper: Soft Error Modeling, Simulation, and Testing at Advanced Technology Nodes
B. L. Bhuva, W. T. Holman, L. W. Massengill
Vanderbilt University, Nashville, TN, USA

Layout Optimization to Maximize Tolerance in SEILA: Soft Error Immune Latch
Taiki Uemura, Tsunehisa Sakoda, Hideya Matsuyama
Fujitsu Semiconductor Ltd., Boulder, Akiruno, Tokyo, Japan

Comparative Analysis of Flip-Flop designs for Soft Errors at Advanced Technology Nodes
B. L. Bhuva1, K. Lilja2, J. Holts3, S.-J. Wen4, R. Wong4, S. Jagannathan1, T. D. Loveless1, M. McCurdy1, Z. J. Diggins1
1Vanderbilt University, Nashville, TN, USA
2Robust Chip, Inc., Pleasanton, CA, USA
3Cisco Systems, Inc. San Jose, CA, USA.

Session N: Emerging Technologies

Invited Paper: Silicon Quantum Well Light-Emitting Diode
S. Saito
Institute for Photonics-Electronics Convergence System Technology (PECST), Photonics Electronics Technology Research Association (PETRA), and Central Research Laboratory, Hitachi, Ltd., Kokubunji, Tokyo, Japan

A Frequency-Shift Readout System for FPW Allergy Biosensor
Chia-Hao Hsu, Yain-Reu Lin, Yue-Da Tsai, Yun-Chi Chen, Chua-Chin Wang, Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan

Invited Paper: Scaled Nanoelectromechanical (NEM) Hybrid Devices
Hiroshi Mizuta1,2, Mario A. Garcia-Ramirez2, Zakaria Moktadir3, Yoshishige Tsuchiya2, Shunichiro Sawai3, Jun Ogi3, Shunri Oda3
1School of Materials Science, Japan Advanced Institute of Science and Technology (JAIST), Ishikawa, Japan
2NANO Group, Electronics and Computer Science, Faculty of Physical and Applied Sciences, University of Southampton, Highfield, Southampton, U.K.
3Quantum Nano Electronics Research, Center, Tokyo Institute of Technology, Ookayama, Meguro-ku, Tokyo, Japan

Evaluation of DC and AC Performance of Junctionless MOSFETs in the Presence of Variability
Xin Qian1, Yinglin Yang1, Zhiwei Zhu1, Shi-Li Zhang1,2, Dongping Wu1
1State Key Laboratory of ASIC and System, Fudan University, Shanghai, People’s Republic of China
2Solid-State Electronics, The Ångström Laboratory, Uppsala University, Uppsala, Sweden