7th International Symposium on Advanced Gate Stack Technology 2010

Albany, New York, USA
29 September - 1 October 2010

7th International Symposium on
Advanced Gate Stack Technology
September 29 - October 1, 2010
Albany, NY

Peering into Moore's Crystal Ball: Transistor Scaling Beyond the 15nm node
Kelin Kuhn, Intel

Electrical Characterization of the III-V and Oxide Interface
Suman Datta, PennState University

Effects of InGaAs Surface Nitridation on InGaAs MOS Interface Properties
Shinichi Takagi, University of Tokyo

Scaling FETs to 10 nm: Coulomb Effects, Source Starvation, and Virtual Source
Massimo Fischetti, University of Texas at Dallas

DFT MD of Defect Passivation by Oxides on III-V and Ge Surfaces
Andrew Kummel, University of California, San Diego

Quantification of Trap State Densities at High-k/III-V Interfaces
Susanne Stemmer, Univ of California, Santa Barbara

III-V Gate Stacks on III-V: New Experimental Results
Serge Oktyabrsky, University at Albany

III-V on Si for VLSI
Richard Hill, SEMATECH

Metal Gate / High-k Reliability Characterization: From Research to Development and Manufacturing
Andres Kerber, GLOBALFOUNDRIES

Understanding of Post-Breakdown Reliability of High-k Gate Dielectric Stacks Using Physical Analysis Techniques
Kin Leong Pey, Singapore University of Technology and Design

Defect Depth Profiling of Gate Dielectric - Some Controversial Points
Kin Wah (Charles) Cheung, NIST

III-V Gate Stack Electrical Characterization
Thomas Hoffmann, IMEC

RRAM Technology From an Industrial Perspective
In-Gyu Baek, Samsung

Charge Trap Memories and 3D Approaches
Gabriel Molas, CEA-LETI

A Survey of Cross Point Phase Change Memory Technologies
DerChang Kau, Intel Corporation

Recent Advancements in Spin-Torque Switching for High-Density MRAM
John Slaughter, Everspin

STT MRAM with High Thermal Stability
Bernard Diény, SPINTEC
<table>
<thead>
<tr>
<th>Title</th>
<th>Author/Institution</th>
<th>Pages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Status and Challenges for Non-Volatile Spin-Transfer Torque RAM (STT-RAM)</td>
<td>Mohamad Krounbi, Grandis</td>
<td>223</td>
</tr>
<tr>
<td>Progress in Metal Oxide RRAM</td>
<td>David Gilmer, SEMATECH</td>
<td>237</td>
</tr>
<tr>
<td>Electrical and Reliability Characteristics of RRAM for Cross-point Memory Applications</td>
<td>Hyunsang Hwang, Gwangju Institute of Science and Technology (GIST), KOREA</td>
<td>247</td>
</tr>
<tr>
<td>Investigation of RRAM Devices for Radiation Harden Applications</td>
<td>Wei Wang, University at Albany</td>
<td>263</td>
</tr>
<tr>
<td>Basics of RRAM based on transition metal oxides</td>
<td>Hisashi Shima, Nanodevice Innovation Research Center</td>
<td>277</td>
</tr>
<tr>
<td>Oxides / Metals for Spin Based Nanoelectronics</td>
<td>Kang Wang, University of California, Los Angeles</td>
<td>290</td>
</tr>
<tr>
<td>Magneto-Electric Coupling at Oxide Interfaces</td>
<td>Alex Demkov, University of Texas at Austin</td>
<td>312</td>
</tr>
<tr>
<td>Tunnel FET Gate-Stack Characterization</td>
<td>Alan Seabaugh, University of Notre Dame</td>
<td>331</td>
</tr>
</tbody>
</table>