2012 IEEE International Conference on IC Design & Technology

(ICICDT 2012)

Austin, Texas, USA
30 May – 1 June 2012
Session A: CAD

**Invited Paper: Design and Analysis of IC Power Delivery with On-chip Voltage Regulation**  
Suming Lai, Peng Li, Zhiyu Zeng  
Texas A&M University, College Station, USA

**Invited Paper: Design Driven Patterning Optimizations for Low K, Lithography**  
Kanak Agarwal, Shayak Banerjee  
1IBM Austin Research Lab, USA  
2IBM Semiconductor Research & Development Center, USA

**Synthesis of Clock Gating Logic through Factored Form Matching**  
Inhak Han, Youngsoo Shin  
KAIST, Daejeon, Korea

**Gate Delay Modeling for Static Timing Analysis of Body-Biased Circuits**  
Donkyu Baek, Insup Shin, Youngsoo Shin  
KAIST, Daejeon, Korea

**A New Statistical Setup and Hold Time Definition**  
Xiaoliang Bai, Prayag Patel, Xiaonan Zhang  
Qualcomm Inc., San Diego, USA

Session B: Reliability / PID

**Invited Paper: Reliability Driven Guideline for BEOL Optimization: Protecting MOS Stacks from Hydrogen-related Impurity Penetration**  
Ziyuan Liu, Fumihiko Hayashi, Shinji Fujieda, Markus Wilde, Katsuyuki Fukutan  
1Device & Analysis Technology Division, Renesas Electronics Corporation, Kanagawa, Japan  
2Smart Energy Research Laboratories, NEC Corporation, Ibaraki, Japan  
3Institute of Industrial Science, University of Tokyo, Tokyo, Japan

**Invited Paper: Superior Reliability and Reduced Time-Dependent Variability in High-Mobility SiGe Channel pMOSFETs for VLSI Logic Applications**  
IMEC, Leuven, Belgium

**Optimization Problems for Plasma-Induced Damage – A Concept for Plasma-Induced Damage Design**  
Koji Eriguchi, Yoshinori Nakakubo, Asahiko Matsuda, Masayuki Kamei, Yoshinori Takao, Kouichi Ono  
Graduate School of Engineering, Kyoto University, Kyoto, Japan

**Impacts of Random Telegraph Noise on the Analog Properties of FinFET and Trigate Devices and Widlar Current Source**  
Chia-Hao Pao, Ming-Long Fan, Ming-Fu Tsai, Yin-Nien Chen, Vita Pi-Ho Hu, Pin Su, Ching-Te Chuang  
National Chiao Tung University, Hsinchu, Taiwan

**Lifetime Prediction of Channel Hot Carrier Degradation in pMOSFETs Separating NBTI Component**  
Y. Mitani, S. Fukatsu, D. Hagishima, K. Matsuzawa  
Advanced LSI Technology Laboratory, Toshiba Corpo., Yokohama, Japan
Session C: Low Power

Invited Paper: Energy Efficient Design Techniques for a Digital Signal Processor
Paul Bassett, Martin Saint-Laurent
Qualcomm Inc., Austin, USA

BAW Filters for Ultra-Low Power Narrow-Band Applications
Carolynn Bernier, Jean-Baptiste David
CEA/LETI, Minatec, Grenoble, France

Design of Low Power, Wider Tuning Range CMOS Voltage Control Oscillator for Ultra Wideband Applications
Iji Ayobami B. Forest Zhu, Michael Heimlich
Macquarie University, Sydney, Australia

32 nm FinFET-based 0.7-to-1.1 V Digital Voltage Sensor with 50mV Resolution
Hung Viet Nguyen, Youngmin Kim
Ulsan National Institute of Science and Technology, Ulsan, Korea

A Low Power Programmable FIR Filter Using Sharing Multiplication Technique
Nahla T. Abou El Kheir¹, Moataz S. El Kharashi¹, Magdy A. El-Moursy²
¹Arab Academy for Science and Technology, Alexandria, Egypt
²Mentor Graphics Corp., Cairo, Egypt

Single-ended Disturb-free 5T Loadless SRAM Cell using 90nm CMOS Process
Sih-Yu Chen, Chua-Chin Wang
National Sun Yat-Sen University, Kaohsiung, Taiwan

Session D: Emerging Technologies

Invited Paper: Low-voltage tunnel transistors: benchmarks and circuits
Alan Seabaugh, D. Jena, S. Kurtz, Y. Lu, Q. Zhang
University of Notre Dame, Notre Dame, USA

System-Level Optimization and Benchmarking of Graphene PN Junction Logic System Based on Empirical CPI Model
Chenyun Pan, Azad Naeemi
Georgia Institute of Technology, Atlanta, USA

Design of Content Addressable Memory Cell using Carbon Nanotube Field Effect Transistor
Debaprasad Das, Avishek Sinha Roy, Hafizur Rahaman, Bhargab B. Bhattacharya
Bengal Engineering and Science University, Shibpur, India

System-Level Design and Performance Modeling for Multilevel Interconnect Networks for Carbon Nanotube Field Effect Transistors
Ahmet Ceyhan, Azad Naeemi
Georgia Institute of Technology, Atlanta, USA

Invited Paper: Nanoscale Power and Heat Management in Electronics
Andrey Y. Serov¹, Zuanyi Li², Kyle L. Grosse², Albert D. Liao¹, David Estrada¹, Myung-Ho Bae¹, Feng Xiong¹, William P. King², Eric Pop³
¹Dept. of Electrical & Computer Engineering
²Dept. of Physics
³Dept. of Mechanical Science & Engineering
University of Illinois, Urbana, USA
Session E: 3D Integration

**Invited Paper: 3D Stacking: Where the Rubber Meets the Road**
Chandra Nimmagadda, Durodami Lisk, Riko Radojcic
Qualcomm, USA

**Evaluation of Non-destructive Etch Depth Measurement for Through Silicon Vias**
Thuy Dao¹, Tania Thomas², David Marx², David Grant²
¹Freescale Semiconductor, Austin, USA
²Tamar Technology, Newbury Park, USA

**Invited Paper: 3D Chip Package Interaction Thermo-mechanical Challenges: Proximity effects of Through Silicon Vias and µ-bumps**
IMEC, Leuven, Belgium

**Analytical Modeling of Parasitics in Monolithically Integrated 3D Inverters**
Joris Lacord¹,², Perrine Batude³, Gerard Ghibaudo², Frederic Boeuf²
¹STMicroelectronics, Crolles, France
²IMEP, Grenoble, France
³CEA-LETI, Grenoble, France

Session F: Advanced Memories

**Invited Paper: Phase-Change Memories for Nano-Scale Technology and Design**
Fabio Pellizzer, Roberto Bez
Micron Technology, Agrate Brianza, Italy

**First-ever High-Performance, Low-Power 32-bit Microcontrollers with Embedded Nanocrystal Flash and Enhanced EEPROM Memories**
Freescale, Austin, USA

A. Kawasumi, Y. Takeyama, O. Hiraibayashi, K. Kushida, F. Tachibana, Y. Niki, S. Sasaki, T. Yabe
Toshiba Corp., Japan

**A 0.32V, 55fJ per bit access energy, CMOS 65nm bit-interleaved SRAM with radiation Soft Error tolerance**
Sylvain Clerc¹, Fady Abouzeid¹, Gilles Gasiot¹, David Gauthier², Dimitri Soussan¹,³, Philippe Roche¹
¹STMicroelectronics, Crolles, France
²EaSi-IC, Grenoble, France
³CEA LETI, Grenoble, France

**Using ECC and Redundancy to minimize VMIN induced Yield Loss in 6T SRAM Arrays**
Guru Shamanna, Raja Gaurav, Raghavendra, Y. K, Percy Marfatia, Bhunesh Kshatri
Intel Corporation, Bangalore, India

Session G: RF & Analog, Mixed signal

**Dynamic Stage Element Matching (DSEM) in Pipeline Analog to Digital Converters (ADC)**
Francis Fradette¹, Eric Balster², Frank Scarpino², Kerry Hill²
¹University of Dayton, Dayton, USA
²Air Force Research Laboratory WPAFB, Ohio, USA
Invited Paper: Temperature and Process Compensated Clock Generator Using Feedback TPC Bias

Tzung-Je Lee1, Doron Shmilovitz2, Yi-Jie Hsieh, Chua-Chin Wang
1Cheng Shiu University, Kaohsiung, Taiwan
2Tel-Aviv University, Tel-Aviv, Israel

Poly-Si Thin Film Transistors: Opportunities for Low-Cost RF Applications
Soo Youn Kim, Wing-Fai Loke, Sang Phill Park, Byunghoo Jung, Kaushik Roy
Purdue University, West Lafayette, USA

Invited Paper: Low-Power Ultra-Wide-Band Impulse Radio Transceivers for Short Range Communications
Andrea Neviani, Andrea Bevilacqua, Andrea Gerosa, Daniele Vogrig
University of Padova, Italy

Session H: Advanced Transistors / Materials

Invited Paper: Emerging CMOS and Beyond CMOS Technologies for ultra-low power 3D World
SEMATECH, USA

Invited Paper: Variability in Fully Depleted MOSFETs
M. Vinet1, T. Hook2, Y. Le Tiec1, R. Murphy2, S. Ponoth1, L. Grenouillet1, R. Wacquez2
1CEA-LETI, France
2IBM, USA

Invited Paper: Strained Silicon on Insulator Substrates for Fully Depleted Application
W. Schwarzenbach, N. Daval, S. Kerdilès, G. Chabanne, C. Fiquet, S. Guerroudj, O. Bonnin, X. Cauchy, B.-Y. Nguyen, C. Maleville
SOITEC, Crolles, France

Robust PEALD SiN spacer for gate first high-k metal gate integration
GLOBALFOUNDRIES, Dresden, Germany

Session I: DFM / DFT / DFR / DFY

Invited Paper: O(n) Mask-Assignment for Multiple Patterning and Removal of Coloring Conflicts Using Compaction
Rani S. Ghaida1, Kanak B. Agarwal2, Sani R. Nassif2, Xin Yuan2, Lars W. Liebmann4, Puneet Gupta1
1UCLA, Electrical Engineering Dept., USA
2IBM Corp., Austin Research Lab, USA
3IBM Corp., San Jose, USA
4IBM Corp., Semiconductor Research & Development Center, USA

Performance Analysis and Modeling of Deep Trench Decoupling Capacitor for 32 nm High-Performance SOI Processors and Beyond
Balaji Jayaraman1, Sneha Gupta1, Yanli Zhang2, Puneet Goyal1, Herbert Ho2, Rishikesh Krishnan2, Sunfei Fang3, Sungjae Lee3, Douglas Daley2, Kevin McStay2, Bernhard Wunder3, John Barth3, Sadanand Deshpande1, Paul Parries3, Rajeev Malik3, Paul Agnello2, Scott Stiffler2, Subramanian S. Iyer2
1IBM Corp., Semiconductor Research and Development Center, Bangalore India,
2IBM Corp., Semiconductor Research and Development Center, Hopewell Junction, USA
3IBM Corp., Semiconductor Research and Development Center, Essex Junction, USA

Ku He, Andreas Gerstlauer, Michael Orshansky
University of Texas, Austin, USA
Unifying Design Data During Verification: Implementing Logic-Driven Layout Analysis and Debug
Kishore Kollu, Trey Jackson, Farhad Kharas, Anant Adke
Mentor Graphics Corporation, Wilsonville, USA

Invited Paper: Spatial Variation Decomposition via Sparse Regression
Wangyang Zhang1, Karthik Balakrishnan2, Xin Li3, Duane Boning3, Emrah Acar3, Frank Liu4, Rob A. Rutenbar5
1Carnegie Mellon University, Pittsburgh, USA
2Massachusetts Institute of Technology, USA
3IBM corp., TJ Watson Lab, USA
4IBM corp., Austin Research Lab, USA
5University of Illinois, Urbana-Champaign, USA

Session J: IO Circuits and ESD Protection

Invited Paper: On-Chip MOS PVT Variation Monitor for Slew Rate Self-Adjusting 2xVDD Output Buffers
Chih-Lin Chen, Hsin-Yuan Tseng, Ron-Chi Kuo, Chua-Chin Wang
National Sun Yat-Sen University, Kaohsiung, Taiwan

A Mixed LPDDR2 Impedance Calibration Technique exploiting 28nm Fully-Depleted SOI Back-Biasing
Dimitri Soussan1,2, Alexandre Valentian2, Sylvain Majcherzak1, Marc Belleville2
1STMicroelectronics, Crolles, France
2CEA LETI, Grenoble, France

BIMOS transistor and its applications in ESD protection in advanced CMOS technology
P. Galy, J. Jimenez, J. Bourgeat, A. Dray, G. Troussier, B. Heitz, N. Guitard, D. Marin-cudraz, H. Beckrich-Ros
STMicroelectronics, Crolles, France

High Swing Low Capacitance ESD RF Protections in Advanced CMOS Technology
Jean Jimenez, Philippe Galy, Johan Bourgeat, Boris Heitz
STMicroelectronics, Crolles, France

Session K: SOC / MPSoC / SIP, SER, & High-Power/High Voltage

Mingoo Seok1, Dongsuk Jeon2, Chaitali Chakrabati3, David Blaauw2, Dennis Sylvester2
1Columbia University, USA
2University of Michigan, USA
3Arizona State University, USA

A High Voltage Analog Multiplexer with Digital Calibration for Battery Management Systems
Chih-Lin Chen1, Yi Hu1, Wayne Luo1, Chua-Chin Wang1, Chun-Ying Juan2
1National Sun Yat-Sen University, Kaohsiung, Taiwan
2Metal Industries Research & Development Centre, Taipei, Taiwan

Minimum Logic of Guaranteed Single Soft Error Resilience Based on Group Distance-Two Code
Bao Liu, Lu Wang
University of Texas, San Antonio, USA

A 1V, Low Power, High-Gain, 3 - 11 GHz Double-Balanced CMOS Sub-Harmonic Mixer
R. Feghhi, S. Naseh