2012 IEEE Silicon Nanoelectronics Workshop

(SNW 2012)

Honolulu, Hawaii, USA
10 – 11 June 2012
Opening Remarks
Sunday, June 10, 8:30
Tsu-Jae King Liu, University of California at Berkeley, General Chair

Session 1: Plenary & Towards Zero Power Electronics
Sunday, June 10, 8:40
Co-chairs: Toshiro Hiramoto, University of Tokyo and Thomas Skotnicki, STMicroelectronics

8:40  1-1  (Plenary Invited) Innovative thermal energy harvesting for zero power electronics, S. Monfray¹, O. Puscasu¹,², G. Savelli², U. Soupremanien², E. Ollier², C. Guerin², L.G. Fréchette³, E. Léveille³, G. Mirshekari³, C. Maitre³, P. Coronel³, K. Domanski³, P. Grabiec⁴, P. Ancy³, D. Guyomar⁵, V. Bottarel⁶, G. Ricotti⁶, F. Boeuf⁴, F. Gaillard⁶, and T. Skotnicki¹, ¹STMicroelectronics, France ²CEA Liten, France ³Université de Sherbrooke, Canada ⁴ITE, Poland, ⁵INSA Lyon, France, ⁶STMicroelectronics, Italy

9:10  1-2  (Plenary Invited) New type steep-S device using the bipolar action, D. Hisamoto, S. Saito, A. Shima, H. Yoshimoto, and K. Torii, Hitachi, Ltd., Japan

9:40  1-3  Experimental Demonstration of Temperature Stability of Si-Tunnel FET over Si-MOSFET, S. Migita, K. Fukuda, Y. Morita, and H. Ota, AIST, Japan

09:55  1-4  Scale laws for enhanced power for MEMS based heat energy harvesting, O. Puscasu¹,², S. Monfray¹, F. Boeuf¹, G. Savelli³, F. Gaillard³, D. Guyomar², T. Skotnicki³, ¹STMicroelectronics, ²INSA Lyon, ³CEA Liten, France

Session 2: Thermal Management & Nanoscale Memory
Sunday, June 10, 10:30
Co-chairs: Byung-Gook Park, Seoul National University and Tsu-Jae King Liu, UC Berkeley

10:30  2-1  (Invited) Energy-Efficiency and Thermal Management in Nanoscale Devices, A.D. Liao, Z.-Y. Ong, A.Y. Serov, F. Xiong, and Eric Pop, University of Illinois at Urbana-Champaign, USA

11:00  2-2  Comparative Study of Tri-Gate- and Double-Gate-Type Poly-Si Fin-Channel Split-Gate Flash Memories, Y.X. Liu¹, T. Kamei², T. Matsukawa¹, K. Endo³, S. O’uchi¹, J. Tsukada¹, H. Yamauchi¹, Y. Ishikawa¹, T. Hayashida², K. Sakamoto¹, A. Ogura², and M. Masahara¹,², ¹AIST ²Meiji University, Japan


A novel Gate-All-Around Ultra-Thin p-channel Poly-Si TFT Functioning as Transistor and Flash Memory with Silicon Nanocrystals, H.-B. Chen, S.-H. Lin, J.-J. Wu, Y.-C. Wu, and C.-Y. Chang, National Chiao Tung University, Taiwan ROC

Session 3: Advanced Channel and Gate Stack Materials
Sunday, June 10, 13:30
Co-chairs: Kristin De Meyer, IMEC and Dong-Won Kim, Samsung Electronics


14:00 3-2 High Performance Ω-Gate Ge FinFET Featuring Low Temperature Si$_2$H$_6$ Passivation and Implantless Schottky-Barrier NiGe Metallic Source/Drain, B. Liu, X. Gong, G. Han, P.S.Y. Lim, Y. Tong, Y. Yang, N. Daval, M. Pulido, D. Delprat, B.-Y. Nguyen, and Y.-C. Yeo, National University of Singapore, Singapore

14:15 3-3 High-performance pMOSFETs with High-k Gate Dielectric and Dislocation-free Epitaxial Si/Ge Super-lattice Channel, L.-J. Liu, K.-S. Chang-Liao, C.-H. Fu, H.-C. Hsieh, C.-C. Lu, T.-K. Wang, P. Y. Gu, and M.J. Tsai, National Tsing Hua University, Industrial Technology Research Institute, Taiwan ROC

14:30 3-4 Counter Dipole Layer Formation in SiO$_2$/High-k/SiO$_2$/Si Gate Stacks, S. Hibino, T. Nishimura, K. Nagashio, K. Kita, and A. Toriumi, University of Tokyo, Japan


15:00 3-6 Transport in Graphene on Boron Nitride, D.K. Ferry, Arizona State University, USA
Session 4: Spintronic Devices
Sunday, June 10, 15:35
Chair: Stephen Goodnick, Arizona State University

15:35  4-1  (Invited) Magnetic Tunnel Junction for Magnetoresistive Random Access Memory and Beyond, H. Ohno, Tohoku University, Japan


16:20  4-3  Analysis of static noise margin and power-gating efficiency of a new nonvolatile SRAM cell using pseudo-spin-MOSFETs, Y. Shuto, S. Yamamoto, and S. Sugahara, Tokyo Institute of Technology, Japan

Poster Session 1: Advanced Memory and Channel Materials
Sunday, June 10, 16:40 – 19:00
Chair: Yee-Chia Yeo, National University of Singapore

16:40  Poster introductions (1 minute each)

Session 5: Emerging Memory Devices
Monday, June 11, 8:30
Co-chairs: Simon Deleonibus, LETI and Malgorzata Jurczak, IMEC

8:30  5-1  (Invited) Recent Progress of Resistive Switching Random Access Memory (RRAM), Y. Wu, S. Yu, X. Guan, and H.-S.P. Wong, Stanford University, USA

9:00  5-2  Bidirectional Selection Device Characteristics of Ultra-Thin (<3nm) TiO2 layer for 3D Vertically Stackable ReRAM Application, J. Woo, J. Park, J. Shin, G. Choi, S. Kim, W. Lee, S. Park, D. Lee, E. Cha, and H. Hwang, University of Science and Technology, Republic of Korea

9:15  5-3  Co-existed Unipolar and Bipolar Resistive Switching Effect of HfOx-Based RRAM, B. Chen, B. Gao, Y.H. Fu, R. Liu, L. Ma, P. Huang, F.F. Zhang, L.F. Liu, X.Y. Liu, J.F. Kang, and G.J. Lian, Peking University, China

9:30  5-4  4kb nonvolatile nanogap memory (NGpM) with 1 ns programming capability, T. Takahashi, S. Furuta, Y. Masuda, S. Kumaragurubaran, T. Sumiya, M. Ono, Y. Hayashi, T. Shimizu, H. Suga, M. Horikawa, and Y. Naitoh, Funai Electric Advanced Applied Technology Research Institute, Tsukuba Device Solution Center, AIST, Japan

9:45  5-5  Characteristics of Metal/Ferroelectric (PVDF-TrFE)/Graphene (MFG) Device, H.J. Hwang, E.J. Paek, J.H. Yang, C.G. Kang, and B.H. Lee, Gwangju Institute of Science and Technology, Korea
Session 6: Single Electron Devices & Quantum Transport
Monday, June 11, 10:20
Co-chairs: Michiharu Tabe, Shizuoka University and Wolfgang Porod, Notre Dame University


10:50  6-2 Reinvestigation of Dot Formation Mechanisms in Silicon Nanowire Channel Single-Electron/Hole Transistors Operating at Room Temperature, R. Suzuki, M. Nozue, T. Saraya, and T. Hiramoto, University of Tokyo, Japan

11:05  6-3 Quantum Transport Property in FETs with Deterministically Implanted Arsenic Ions Using Single-ion Implantation, M. Hori, T. Shinada, F. Guagliardo, G. Ferrari, and E. Prati, Waseda University, Japan Politecnico di Milano, CNR-IMM, Italy

11:20  6-4 High-frequency properties of Si single-electron transistor, H. Takenaka, M. Shinhara, T. Uchida, M. Arita, A. Fujiwara, Y. Ono, K. Nishiguchi, H. Inokawa, and Y. Takahashi, Hokkaido University, Japan


11:50  6-6 Mapping of single donors in nano-scale MOSFETs at low temperature, J. Vertudijn, G.C. Tettamanzi, R. Wacquez, B. Roche, B. Voisin, X. Jehl, S. Rogge, University of New South Wales, Australia Delft University of Technology, The Netherlands CEA-LETI, France

Session 7: Nanoscale Phenomena
Monday, June 11, 13:30
Co-chairs: Kazuhiko Endo, AIST and Yukinori Ono, University of Toyama

13:30  7-1 (Invited) A Single Atom Transistor, M.Y. Simmons, University of New South Wales, Australia

14:00  7-2 Statistical Variability Study of a 10nm Gate Length SOI FinFET Device, B. Cheng, A.R. Brown, X. Wang, and A. Asenov, University of Glasgow Gold Standard Simulations, United Kingdom

14:15  7-3 Reduced Drain Current Variability in Fully Depleted Silicon-on-Thin-BOX (SOTB) MOSFETs, T. Mizutani, Y. Yamamoto, H. Makiyama, T. Tsunomura, T. Iwamatsu, H. Oda, N. Sugii, and T. Hiramoto, University of Tokyo Low-power Electronics Association & Project, Japan

14:30  7-4 The Impact of the Carrier Transport on the Random Dopant Induced Drain Current Variation in the Saturation Regime of Advanced Strained-Silicon CMOS Devices, E.R. Hsieh, S.S. Chung, C.H. Tsai, R.M. Huang, C.T. Tsai, and C.W. Liang, National Chiao Tung University United Microelectronics Corporation, Taiwan ROC
14:45  7-5  On the Statistical Trap-Response (STR) Method for Characterizing Random Trap Occupancy and NBTI Fluctuation, J. Zou, C. Liu, R. Wang, X. Xu, J. Liu, H. Wu, Y. Wang, R. Huang, Peking University, Semiconductor Manufacturing International Corporation, China

15:00  7-6  Statistical distribution of RTS amplitudes in 20nm SOI FinFETs, X. Wang, A.R. Brown, B. Cheng, and A. Asenov, University of Glasgow, Gold Standard Simulations, United Kingdom

**Poster Session 2: Nanoscale/Quantum Devices and Phenomena**
Monday, June 11, 15:20 – 17:30
Chair: Thomas Skotnicki, STMicroelectronics
15:20  **Poster introductions** (1 minute each)

**Poster Session 1: Advanced Memory and Channel Materials**
Sunday, June 10, 16:40 – 19:00

**P1-1** Self-Improvement of Cell Stability in SRAM by Post Fabrication Technique, A. Kumar, T. Saraya, S. Miyano, and T. Hiramoto, University of Tokyo, Japan


**P1-3** Low Standby Power Charge Trap Flash Memory with Tunneling Field Effect Transistor, M.S. Han, J.H. Lee, D. Seo, C.-D. Park, Y. Oh, and I.H. Cho, Myongji University, Seoul National University, Korea

**P1-4** Charge-trap flash memory devices fabricated with nano-scale patterns on the Si3N4 trapping layer, H.-M. An, K.H. Kim, H.-D. Kim, W.-J. Cho, and T.G. Kim, Korea University, Kwangwoon University, Korea

**P1-5** Simulation of Charge Trapping Memory with Silicon Nanocrystals Embedded in Silicon Nitride Layer, Y. Peng, X. Liu, G. Du, Y. Yang, and J. Kang, Peking University, China

**P1-6** Nanodot-type Floating Gate Memory with High-density Nanodot Array Formed Utilizing Listeria Dps, H. Kamitake, K. Ohara, M. Uenuma, B. Zheng, Y. Ishikawa, I. Yamashita, and Y. Uraoka, Nara Institute of Science and Technology, Panasonic Corporation, Japan

**P1-7** Impacts of Silicon Nanocrystal Incorporation on the Transfer Characteristics of Poly-Silicon nanowire SONOS Devices, K.-H. Lee, H.-C. Lin, and T.-Y. Huang, National Chiao Tung University, Taiwan ROC


P1-10 Self-compliance Unipolar Resistive Switching and Mechanism of Cu/SiO₂/TiN RRAM Devices, D. Yu, L.F. Liu, P. Huang, F.F. Zhang, B. Chen, B. Gao, Y. Hou, D.D. Han, Y. Wang, J.F. Kang, and X. Zhang, Peking University, China

P1-11 Stable Resistive Switching Characteristics Observed in SiN-based Resistive Switching Memory Devices by using RF-sputtering methods, H.-D. Kim, S.M. Hong, H.-M. An, K.H. Kim, Y. Seo, M. Song, D. Li, and T.G. Kim, Korea University, Korea

P1-12 Rectifying Characteristics and Implementation of n-Si/HfO₂ based Devices for 1D1R-based Cross-Bar Memory Array, F. F. Zhang, P. Huang, B. Chen, D. Yu, Y.H. Fu, L. Ma, B. Gao, L.F. Liu, X.Y. Liu, and J.F. Kang, Peking University, China

P1-13 Oxygen-induced High-k Degradation in TiN/HfSiO Gate Stacks, T. Hosoi, Y. Odate, K. Chikaraishi, H. Arimura, N. Kitano, T. Shimura, and H. Watanabe, Osaka University, Japan

P1-14 Metal/Ge Schottky Barrier Modulation With C-Containing Layer by Chemical Bath, W. Wang, J. Wang, M. Zhao, R. Liang, and J. Xu, Tsinghua University, China

P1-15 Orientation and Size Effects on Ballistic Electron Transport Properties in Gate-All-Around Rectangular Germanium Nanowire FETs, S. Mori, N. Morioka, J. Suda, and T. Kimoto, Kyoto University, Japan

P1-16 Quantum Transport Simulation of III-V MOSFETs based on Wigner Monte Carlo Approach, Y. Maegawa, S. Koba, H. Tsuchiya, and M. Ogawa, Kobe University, Japan


P1-18 Electronic Band Structures of Graphene Nanomeshes, R. Sako, N. Hasegawa, H. Tsuchiya, and M. Ogawa, Kobe University, Japan

P1-19 Band Structure and Electron Transport in Multi-Junction Graphene Nanoribbons, N. Hasegawa, R. Sako, H. Tsuchiya, and M. Ogawa, Kobe University, Japan

P1-20 Graphene-Diamond-Silicon Devices with Increased Current-Carrying Capacity: sp²-Carbon-on-Silicon Technology, J. Yu¹, G. Liu¹, A.V. Sumant³, and A. A. Balandin¹, University of California at Riverside, Argonne National Laboratory, USA

P1-21 Selective Gas Sensing with a Single Graphene-on-Silicon Transistor, A.A. Balandin¹, S. Rumyantsev², S. Liu¹, M.S. Shur², and R.A. Potyrailo³, University of California at Riverside, Rensselaer Polytechnic Institute, GE Global Research, USA

P1-22 Graphene Fillers for Ultra-Efficient Thermal Interface Materials, K.M.F. Shahil, V. Goyal, R. Gultoty, and A.A. Balandin, University of California at Riverside, USA

Poster Session 2: Nanoscale/Quantum Devices and Phenomena

Monday, June 11, 15:20 – 17:30

P2-1 Simulation Study on Process Conditions for High-Speed Silicon Photodetector and Quantum-Well Structuring for Increased Number of Wavelength Discriminations, S. Cho¹, H. Kim², M.-C. Sun², T.I. Kamins¹, B.-G. Park², and J.S. Harris, Jr.¹, Stanford University, USA ²Seoul National University, Korea

P2-2 Nano-Transfer Printing of Functioning MIM Tunnel Diodes, Mario Bareiß¹, B. Weißer¹, D. Källblein², U. Zschieschang², H. Klauk², G. Scarpa¹, B. Fabel¹, P. Lugli³, and W. Porod³,¹Technische Universität München, Germany ²Max Planck Institute for Solid State Research, Germany ³University of Notre Dame, USA

P2-3 Fabrication and evaluation of heavily P-doped Si quantum dot and back-gate induced Si quantum dot, J. Kamioka¹, T. Kodera¹-², K., Horibe¹, Y. Kawano¹, and S. Oda¹,¹Tokyo Institute of Technology ²University of Tokyo Japan

P2-4 Microwave manipulation of electrons in silicon quantum dots, T. Ferrus¹, A. Rossi¹, T. Kodera²-³, T. Kambara², W. Lin², S. Oda², and D.A. Williams¹,¹Hitachi Cambridge Laboratory, United Kingdom ²Tokyo Institute of Technology ³University of Tokyo Japan

P2-5 Charge sensing of a Si triple quantum dot system using single electron transistors, R. Mizokuchi, T. Kodera, K. Horibe, Y. Kawano, and S. Oda, Tokyo Institute of Technology, Japan

P2-6 Fabrication and characterization of Si/SiGe quantum dots with capping gate, T. Kodera¹-², Y. Fukuoka¹, K. Takeda², T. Obata², K. Yoshida², K. Sawano², K. Uchida¹, Y. Shiraki³, S. Tarucha², and S. Oda¹, Tokyo Institute of Technology ²University of Tokyo ³Tokyo City University, Japan

P2-7 Single Ge quantum dot placement along with self-aligned electrodes for effective management of single electron tunneling, I. H. Chen, K. H. Chen, and P. W. Li, National Central University, Taiwan ROC

P2-8 Single-electron transport through a single donor at elevated temperatures, E. Hamid, D. Moraru, T. Mizuno and M. Tabe, Shizuoka University, Japan

P2-9 The Interplay of Self-Heating Effects and Static RTF in Nanowire Transistors, D. Vasileska, A. Hossain, and S.M. Goodnick, Arizona State University, USA

P2-10 Effect of Interfacial States on the technological variability of Trigate MOSFETs, E. González-Marín, F.G. Ruiz, A. Godoy, I.M. Tienda-Luna, F. Gámiz, Universidad de Granada, Spain

P2-11 Evolution of Channel Trap Distribution under Bias Stress in Polysilicon Thin Film Transistors evaluated by Charge Pumping Method, C.N. Manh¹, J.S. Chang¹, T.-Y. Jang¹, M. Hasan¹, H. Yang¹, J.K. Jeong¹, B. Kim¹, J. Ahn², K. Hwang², and R. Choi¹,¹Inha University ²Samsung Electronics Co., Ltd., Korea

P2-12 Physical Model for Random Telegraph Noise Amplitudes and Implications, R.G. Southwick III¹, K.P. Cheung¹, J.P. Campbell¹, S.A. Drozdov², J.T. Ryan¹, J.S. Suehle¹, and A.S. Oates³,¹National Institute of Standards and Technology, ²University of Maryland USA ³Taiwan Semiconductor Manufacturing Company Ltd., Taiwan ROC
P2-13 Optoelectrical Lifetime Evaluation of Single Holes in SOI MOSFET, W. Du\textsuperscript{1}, D.S. Putranto\textsuperscript{1,2}, H. Satoh\textsuperscript{1}, A. Ono\textsuperscript{1}, P.S. Priambodo\textsuperscript{2}, D. Hartanto\textsuperscript{2}, and H. Inokawa\textsuperscript{1}
\textsuperscript{1}Shizuoka University, Japan \textsuperscript{2}University of Indonesia, Indonesia

P2-14 Ab initio analysis of donor state deepening in Si nano-channels, D. Moraru\textsuperscript{1}, Y. Putranto\textsuperscript{1}, Kuzuya\textsuperscript{1}, E. Hamid\textsuperscript{1}, T. Mizuno\textsuperscript{1}, M. Tabe\textsuperscript{1}, and H. Mizuta\textsuperscript{2}, \textsuperscript{1}Shizuoka University, Japan \textsuperscript{2}University of Southhampton, United Kingdom

P2-15 Channel Length-Dependent Series Resistance?, J.P. Campbell\textsuperscript{1}, K.P. Cheung\textsuperscript{1}, S.A. Drozdov\textsuperscript{2}, R.G. Southwick\textsuperscript{1}, J.T. Ryan\textsuperscript{1}, A.S. Oates\textsuperscript{3}, J.S. Suehle\textsuperscript{1}, \textsuperscript{1}National Institute of Standards and Technology, \textsuperscript{2}University of Maryland USA \textsuperscript{3}Taiwan Semiconductor Manufacturing Company Ltd., Taiwan ROC

P2-16 Effects of Amorphous Silicon Atomic Density Variation on Series and Contact Resistances in Nanoscale Thin-Film Structures, M.W. Ryu, S.-H. Kim, and K.R. Kim, Ulsan National Institute of Science and Technology, Korea

P2-17 Evaluation of Scattering in Asymmetric Quasi-Ballistic DG-MOSFET, G. Liu, G. Du, T. Lu, X. Liu, P. Zhang, and X. Zhang, Peking University, China

Fabrication and Characterization of a Pi-Gate Ultrathin Body Junctionless poly-Si TFTs J. Wu, H. Chen, M. Han, Y. Wu, C. Chang

P2-18 Orientational and Si-SiO\textsubscript{2} roughness topology dependence of electron mobilities in silicon gate-all-around nanowire FETs, M. Bescond and E. Dib, Technologies Château-Gombert, France

P2-19 Junctionless poly-Si TFTs, J.-J. Wu\textsuperscript{1}, H.-B. Chen\textsuperscript{1}, M.-H. Han\textsuperscript{1}, Y.-C. Wu\textsuperscript{2}, and C.-. Chang\textsuperscript{1}, \textsuperscript{1}National Chiao Tung University \textsuperscript{2}National Tsing Hua University, Taiwan ROC

P2-20 Quantum Drift-Diffusion and Quantum Energy Balance Simulation of Nanowire Junctionless Transistors, O. Badami, N. Kumar, D. Saha, and S. Ganguly, Indian Institute of Technology Bombay, India

P2-21 Characteristics and Sensitivity of p-Type Junctionless Gate-All-Around Nanowire Transistor, M.-H. Han\textsuperscript{1}, Y.-R. Jhan\textsuperscript{2}, J.-J. Wu\textsuperscript{1}, H.-B. Chen\textsuperscript{1}, Y.-C. Wu\textsuperscript{2}, and C.-Y. Chang\textsuperscript{1}, \textsuperscript{1}National Chiao Tung University \textsuperscript{2}National Tsing Hua University, Taiwan ROC

P2-22 Analysis of Hysteresis Characteristics of Fabricated SiNW Biosensor in Aqueous Environment with Reference Electrode, J.H. Lee\textsuperscript{1}, J. Lee\textsuperscript{2}, M.-C. Sun\textsuperscript{1}, W.H. Lee\textsuperscript{2}, M. Uhm\textsuperscript{2}, S. Hwang\textsuperscript{2}, I.-Y. Chung\textsuperscript{1}, D.M. Kim\textsuperscript{2}, D.H. Kim\textsuperscript{2}, and B.-G. Park\textsuperscript{1}, \textsuperscript{1}Seoul National University \textsuperscript{2}Kookmin University \textsuperscript{3}Kwangwoon University

P2-23 Investigation on Hump Effects of L-shaped Tunneling Field-Effect Transistors, S.W. Kim\textsuperscript{1}, W.Y. Choi\textsuperscript{2}, H. Kim\textsuperscript{1}, M.-C. Sun\textsuperscript{1,3}, H. W. Kim\textsuperscript{1}, and B.-G. Park\textsuperscript{1}, \textsuperscript{1}Seoul National University \textsuperscript{2}Sogang University \textsuperscript{3}Samsung Electronics Co., Ltd., Korea

P2-24 Device Structure for the Characterization of Nanowire Thermocouples, G.P. Szakmany, P.M. Krenz, A.O. Orlov, G.H. Bernstein, and W. Porod, University of Notre Dame, USA