2012 13th Latin American Test Workshop

(LATW 2012)

Quito, Ecuador
10 – 13 April 2012
Wednesday, April 11th 2012

08:30 – 09:00  TTEP Tutorials and LATW Registration

09:00 – 09:20  LATW Opening Session

9:20 – 10:10  KEYNOTE ADDRESS: On-Chip Structures for Parametric Test
               Presenter: Jacob Abraham, University of Texas at Austin, USA

10:10 – 10:40  Coffee break

10:40 – 11:40  SESSION 1: Fault Analysis, Simulation and Diagnosis
               Session Chair: Fabian Vargas, Catholic University of Rio Grande do Sul (PUCRS), Brazil

   Built-in Self-Diagnosis Targeting Arbitrary Defects with Partial Pseudo-Exhaustive Test  1
   Alejandro Cook, Michael Imhof, Abdullah Mumtaz, Hans-Joachim Wunderlich – University of Stuttgart,
   Sybille Hellebrand – University of Paderborn

   Simulation of SET Faults in a Voltage Controlled Oscillator  5
   Walter Calienes bartra, Fernanda Kastensmidt, Ricardo Reis – UFRGS

   Low Voltage Testing for Interconnect Opens under Process Variations  11
   Jesus Moreno, Victor Champac – Inaoe, Michel Renovell – Universite de Montpellier II

11:40 – 12:20  SPECIAL SESSION 1: Robust and Testable Designs in the Nano-Regime
               Organizer: Kaushik Roy, Purdue University, USA

   Low-Power Design under variation using error prevention and error tolerance  17
   Kwanyeob Chae, Saibal Mukhopadhayay – Georgia Institute of Technology

   Variation-aware and self-healing design methodology for a system-on-chip  23
   Jangjoon Lee, Srikan Bhaggavatula, Kaushik Roy, Byunghoo Jung – Purdue University

12:20 – 14:00  Lunch and TTEP Registrations

14:00 – 15:30  Test Technology Educational Program (TTEP)

   TTEP 1:  Statistical Adaptive Test Methods Targeting “Zero Defect” IC Quality and Reliability
            Presenter: Adit D. Singh, Auburn University, USA
            Email: adsingh@auburn.edu

   TTEP 2:  Design for Yield and Reliability
            Presenter: Yervant Zorian, Synopsys, USA
            Email: Yervant.Zorian@synopsys.com

15:30 – 16:00  Coffee break

16:00 – 17:30 Test Technology Educational Program (TTEP)

20:30 – 22:00  Welcome Reception
Thursday, April 12th 2012

09:00 – 09:30 INVITED TALK: Designing RFID Chips for Test & Security: Towards a Reliable Internet of Things
Presenter: Marcelo Lubaszewski, CEITEC S.A., Brazil

09:30 – 10:30 SESSION 2: Design Verification and Validation
Session Chair: Florence Azais, LIRMM, France

Diagnosis and correction of multiple design errors using critical path tracing and mutation analysis  
Hanno Hantson, Urmas Repinski, Jaan Raik, Maksim Jenihhin, Raimund Ubar – Tallinn University of Technology

A Guiding Heuristic for the Semi-Formal Verification of High-Level Designs  
Alair Dias Junior, Diógenes Silva Junior – Federal University of Minas Gerais

Manipulation of Training Sets for Improving Data Mining Coverage-Driven Verification  
Edgar Romero, Marius Strum, Jiang Chau Wang – University of Sao Paulo

10:30 – 10:50 Coffee break

10:50 – 11:30 SESSION 3: Design Optimization
Session Chair: Francisco Russi, Synopsys, USA

Self-Optimization of Dense Wireless Sensor Networks based on Simulated Annealing  
Alex Roschildt Pinto, Adriano Cansian, José Machado – universidade estadual paulista, Carlos Montez – Universidade Federal de Santa Catarina

Design-for-manufacturability of MEMS convective accelerometers through adaptive electrical calibration strategy  
Ahmed Rekik, route soukra, Florence Azais, Frederick Mailly, Pascal Nouet – Univ. Montpellier

11:30 – 12:30 SESSION 4: Product Quality and Software Testing
Session Chair: Adit D. Singh, Auburn University, USA

Investigating the Use of An On-Chip Sensor to Monitor NBTI Effect in SRAM  
Arthur Ceratti, Thiago Copetti, Leticia Bolzani Poehls, Fabian Vargas – Catholic University

Parametric DC and Noise Measurements for a Unified Production Line Characterization Framework Software Tool  

Mutation Operators for Concurrent Programs in MPI  
Rodolfo Silva, Simone Souza, Paulo Souza – Universidade de Sao Paulo

12:30 – 14:30 Lunch Break

14:30 – 15:30 SESSION 5: Automatic Test Generation
Session Chair: Vishwani Agrawal, Auburn University, USA

Automatic generation of an FPGA based embedded test system for printed circuit board testing  
Jorge Hernan Meza Escobar, Jörg Sachsse, Steffen Ostendorff, Heinz-Dietrich Wuttke – Ilmenau University of Technology

Platform for Automated HW/SW Co-verification, Testing and Simulation of Microprocessors  
Aleksandar Simevski, Rolf Kraemer – Brandenburg University of Technology, Milos Krstic – IM Technologiepark
About Robustness of Test Patterns Regarding Multiple Faults  80
Raimund Ubar, Sergei Kostin, Jaan Raik – Tallinn University of Technology

15:30 – 16:30 SPECIAL SESSION 2: Power- and Thermal-Aware Modeling and Design
Organizer: Jose Ayala, Complutense University of Madrid, Spain

Model-Based Design for Wireless Body Sensor Network Nodes  86
Ivan Beretta, David Atienza – Embedded Systems Laboratory, Francisco Rincon – Universidad Complutense de Madrid, Nadia Khaled, Paolo Roberto Grassi, Vincenzo Rana, Donatella Sciuto – Politecnico di Milano

Fast and Scalable Temperature-driven Floorplan Design in 3D MPSoCs  92
Ignacio Arnaldo, J. Ignacio Hidalgo, Jose L. Ayala, Jose L. Risco – Complutense University Madrid, Alessandro Vicenzi, Martino Ruggiero, David Atienza – EPFL

Fast Worst-Case Peak Temperature Evaluation for Real-Time Applications on Multi-Core Systems  98
Lars Schor, Iuliana Bacivarov, Hoeseok Yang, Lothar Thiele – ETH ZURICH

16:30 – 17:00  Coffee break

17:00 – 17:40 SESSION 6: Analog and Mixed Signal Circuits
Session Chair: Marcelo Lubaszewski, Federal University of Rio Grande do Sul (UFRGS), Brazil

Built-in Tunning of RFIC Passive Polyphase Filter by Process and Thermal Monitoring  104
Fayrouz Haddad, Wenceslas Rahajandraibe, Hassen Azza, Karine Castellani-Coulie, Jean Michel Portal – Aix Marseille UNIVERSITY

Multi-condition alternate test of analog, mixed-signal, and RF systems  109
Manuel Barragan, Gildas Leger, Jose Luis Huertas – UNIVERSIDAD DE SEVILLA

20:00 – 23:00  Gala Dinner

Friday, April 13th 2012

09:00 – 09:30 INVITED TALK: Pre-Computed Asynchronous Scan
Presenter: Vishwani Agrawal, Auburn University, USA

09:30 – 10:10 SPECIAL SESSION 3: Thermal Aware Design and Test
Organizer: Marta Rencz, Technical University of Budapest, Hungary

Acquiring real-time heating of cells in standard cell designs  115
Andras Timar, Marta Rencz – BUDAPEST UNIVERSITY OF TECHNOLOGY AND ECONOMICS

Simulation Framework for Multilevel Power Estimation and Timing Analysis of Digital Systems Allowing the Consideration of Thermal Effects  120
Gergely Nagy, András Poppe – BUDAPEST UNIVERSITY OF TECHNOLOGY AND ECONOMICS

10:10 – 10:40  Coffee break

10:40 – 11:40 SESSION 7: Design and Synthesis for Testability
Session Chair: Fernanda Kastensmidt, Federal University of Rio Grande do Sul (UFRGS), Brazil

PSL Assertion Checkers Synthesis with ASM Based HLS tool ABELITE  125
Maksim Jenihhin, Jaan Raik, Valentin Tihhomirov-TtALLINN UNIVERSITY OF THETECHNOLOGY, Samary Baranov – BAR ILAN UNIVERSITY

Retiming Scan Circuit to Eliminate Timing Penalty  131
Ozgur Sinanoglu – NEW YORK UNIVERSITY ABU DHABI, Vishwani Agrawal – AUBURN UNIVERSITY

IEEE STD 1149.1 Basics and Advance Topics, FRANCISCO RUSSI – SYNOPSIS

11:40 – 12:40 SESSION 8: Harsh Environments: Radiation and EMI
Session Chair: Hervé Lévi, University of Bordeaux 1, France
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**Saturday, April 14th 2012**

Department to Galapagos

**Monday, April 16th 2012**

19:00 – 20:00 PANEL SESSION: Challenges of Advanced Nanotechnologies to Test Development