

2012 19th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits

(IPFA 2012)

**Singapore
2 – 6 July 2012**



**IEEE Catalog Number: CFP12777-PRT
ISBN: 978-1-4673-0980-6**

TABLE OF CONTENTS

Lock-in IR-OBIRCH Assisted with Current Detection Probe Head Extend Its Application to High Voltage High Current Failure Analysis	1
<i>C. Wu, L. Tian, M. Wu, D. Fan</i>	
Die-Level Leakage Current Path Analysis Based on IR-OBIRCH Technology	5
<i>J. Li, G. Wen, J. Yu, G. Song</i>	
Diffusion Ability Of Stress Induced Voiding In Advanced BEOL Copper Process	9
<i>C. Huang, J. Liang, A. Juan, K. Su</i>	
C-AFM Analysis of Advanced IC on SRAM High Resistance Failure	12
<i>W. Leong, H. Zhang, W. Hoe, R. Lin</i>	
TEM Sample Preparation by Single-sided Low-energy Ion Beam Etching	15
<i>L. Nan, L. Lung</i>	
Copper Wirebond Package Decapsulation Technique Using Mixed Acid Chemistry	18
<i>S. Ng, H. Zhang, K. Liew, W. Lee, R. Lin</i>	
Noble Failure Analysis Procedure for Trench MOSFET Technology Devices Through Detail Electrical Parameter Characterization and Unique Fault Isolation Technique	23
<i>A. Yahya, N. Yusof, Y. Yusof</i>	
Interface Trap Distribution for HCI Reliability Assessment on Bend Gate Structure by 3D TCAD Simulation	29
<i>B. Prabowo, S. Amethystna, J. Tsai, S. Yang, G. Sheu</i>	
A Practical TEM Sample Preparation Method For Dopant Profile Delineation In Vertical Nanowire Tunneling FETs	33
<i>L. Tang, Y. Zhang, A. Trigg, X. Li</i>	
Investigation of Electrochemical Migration on Fine Pitch BGA Package	37
<i>Y. Chen, M. Hsiao</i>	
A Temperature Control Solution Applied to IC Failure Analysis at Low Temperature	41
<i>J. Li, J. Liu</i>	
Reliability Properties Comparison for Epitaxy and Non-Epitaxy Wafers on DRAM Devices	45
<i>Y. Chen, C. Chen, M. Hsiao</i>	
Applications of C-AFM Technique to Identify Localized Implant Related Low Yield Issue	49
<i>S. Hong, Z. Hua, A. Chin, C. Guan</i>	
Thermal Analysis of AlGaN/GaN High-Electron-Mobility Transistors by Infrared Microscopy	53
<i>M. Zhao, X. Liu, Y. Zheng, K. Wei, M. Peng, Y. Li, G. Liu</i>	
Failure Analysis of Damaged Dielectric on Resistor and Capacitor with EMMI and IR-OBIRCH	57
<i>L. Tian, M. Wu, D. Fan, C. Wu, G. Wen, D. Wang</i>	
Surface Potential and Electric Field Mapping of p-well/n-well Junction by Secondary Electron Potential Contrast and In-situ Nanoprobe Biasing	61
<i>J. Lee, P. Liu, M. Wang, Y. Lin, Y. Huan, D. Su</i>	
Alternative FIB Cross Section and Laser Ablation Methods to Improve Failure Analysis Throughput of Copper Wire Moisture Related Reliability Failures	64
<i>W. Kho, J. Leow, Y. Cheah</i>	
On The Fly Oxide Trap (OTFOT) Concept: A New Method for Bias Temperature Instability Characterization	68
<i>B. Djezzar, H. Tahi, A. Benabdelmoumene, F. Hadjlarbi, A. Chenouf</i>	
New and Novel Failure Analysis Technique of COL Package Device with WBC Non Conductive Epoxy and The Failure Mechanisms of The Electrical Shorting of The Die Back To The Lead	73
<i>Z. Lau, H. Foo, Y. Yusof, Y. Lee, L. Law</i>	
Innovative Methodology for Failure Rate Estimation from Quality Incidents, for ISO26262 Standard Requirements	79
<i>C. Berges, Y. Chandon, R. Gubian</i>	
Reliability Analysis of CrSi Thin Film Resistors	85
<i>C. Khor, C. Leung, O. Neel</i>	
Failure Analysis on Gate-Driven ESD Clamp Circuit after TLP Stresses of Different Voltage Steps in a 16-V CMOS Process	89
<i>C. Dai, P. Chiu, M. Ker, F. Tsai, Y. Peng, C. Tsai</i>	
Power MOSFET Breakdown Voltage Study for Process Control by SIMS	93
<i>K. Ong, L. Zhu, Y. Huang, Y. Hua, S. Oh, Z. Liu</i>	

Failure Analysis on Plasma Charging Induced Damage due to Effect of Circuit Layout & Device Structure Marginality	96
<i>F. Chow, A. Chin</i>	
Au/Pt/Ti-Si₃N₄ Interfacial Defects Analysis Of A Stressed SiGe HBT by using STEM Nanometric Characterization	101
<i>A. Alaeddine, C. Genevois, L. Chevalier, K. Daoud</i>	
TID Characterization Of 0.13µm SONOS Cell In 4Mb NOR Flash Memory	105
<i>F. Qiao, X. Yu, L. Pan, H. Ma, D. Wu, J. Xu</i>	
Quantitative Investigation Of The Adhesion Failure Of Ti-Based Metal Thin Films On Si Wafers	109
<i>S. Chen, J. Zhu, A. Du, Y. Hua</i>	
Impact Of Line Width On Hydrostatic Stress And Stress-Induced Voiding In Cu Interconnects	113
<i>H. Guo, L. Chen</i>	
TEM Dark-Field Off-Axis Electron Holography Strain Measurement on Embedded-SiGe pMOSFETs and Comparison with Nano-Beam Diffraction Strain Measurement	117
<i>J. Zhu, Y. Zhou, S. Toh, Z. Mai, J. Lam, A. Du, Y. Hua, R. Rajgopal</i>	
Case Studies On Application Of Time Resolved Imaging Emission Microscopy For Backside Timing Analysis.....	122
<i>A. Uchikado, S. Kawanab, T. Okubo, A. Shimase, T. Majima, N. Hirai, Y. Ito, T. Nakamura</i>	
Failure Analysis on Ultra-low K Film De-lamination by TOF-SIMS Composition Analysis	126
<i>H. Teo, S. Chen, L. Zhu, Y. Hua, Z. Yuan, Y. Heng, C. Li</i>	
Scrubber Clean Induced Device IDDQ Fail	129
<i>R. Chiu, J. Higgins, S. Ying, S. Chang, J. Chung, B. Dick, E. Lee</i>	
Fault Localization Using IR Lock-in Thermography for Flashover Between the Gate Rail and the Source Metal Clip	133
<i>C. Lau</i>	
A Novel Internal Field Enhanced Retention Degradation Model for Localized Charge Trapping Memory Device	137
<i>X. Yu, L. Pan, F. Qiao, G. Shi, J. Xu</i>	
EELS Chemical Bond Characterization of Process Induced Damages in Low-k Dielectric Films	141
<i>Y. Zhou, J. Zhu, A. Du, Y. Hua, S. Zhao, W. Liu, F. Zhang, J. Tan</i>	
Laser Voltage Probing in Failure Analysis of Advanced Integrated Circuits on SOI	146
<i>V. Ravikumar, R. Wampler, M. Ho, J. Christensen, S. Phoa</i>	
Characterization and TCAD Simulation of 90 nm Technology Transistors Under Continous Photoelectric Laser Stimulation for Failure Analysis Improvement	150
<i>R. Llido, A. Sarafianos, O. Gagliano, V. Serradeil, V. Goubier, M. Lisart, G. Haller, V. Pouget, D. Lewis, J. Dutertre, A. Tria</i>	
Electrical And Charge Trapping Properties of HfO₂/Al₂O₃ Bilayer Gate Dielectrics On In_{0.53}Ga_{0.47}As Substrates	156
<i>A. Ghosh, T. Das, C. Mukherjee, A. Bandyopadhyay, G. Dalapati, D. Chi, C. Maiti</i>	
Failure Analysis Challenges and Solution for Thin Package	160
<i>V. Ben, W. Chan, A. Idayu, H. Heng</i>	
Low Frequency Noise in Iron Disilicide Heterojunction Solar Cells	165
<i>A. Bag, C. Mukherjee, S. Mallik, C. Maiti</i>	
Advanced Fault Isolation Technique Using Electro-optical Terahertz Pulse Reflectometry	169
<i>M. Tay, L. Cao, M. Venkata, L. Tran, W. Donna, W. Qiu, J. Alton, P. Taday, M. Lin</i>	
Studies on Lattice Vibration, Impurity and Defects in MIS Structures Using Hf-based Dielectrics on Si and SiGe Substrates	174
<i>C. Mukherjee, S. Mallik, M. Hota, T. Das, C. Maiti</i>	
Improved Failure Analysis in 3D Electronic Packages by MicroCT	178
<i>H. Roth, T. Neubrand</i>	
Shifting Time Waveform Induced CMOS Latch Up in Bootstrapping Technique Applications	183
<i>Purwadi, S. Bai, B. Prabowo, J. Tsai, G. Sheu</i>	
Ab Initio Method for Electromigration Analysis	187
<i>H. Ceric, R. Orio, W. Zisser, S. Selberherr</i>	
Case Studies of Laser Ablation Effects on Flash Memory Devices.....	191
<i>Y. Seng, Y. Chai, C. Cheng, S. Li</i>	
High Reliability Gold based Solder Alloys for Micro-electronics Packaging for High Temperature Applications.....	195
<i>V. Yeung, G. Shan</i>	
Correlation of Very Fast Transmission Line Pulse (VFTLP) and Field-Induced Charged Device Model (CDM) Testing.....	201
<i>Y. Xue</i>	

Color Guided Top Down Analysis On Memory Device	204
<i>Y. Khong, F. Yong</i>	
Space Domain Reflectometry for Open Failure Localization	208
<i>J. Gaudestad, V. Talanov, N. Gagliolo, A. Orozco</i>	
Analysis of Data Pad Open Failure	213
<i>H. Yang, J. Lee, G. Han, S. Han, D. Oh</i>	
Failure Analysis On The Standby Current Due To Dislocation In STI Structure Of Flash Memory	216
<i>S. Kim, H. Yang, S. Yang, J. Ahn, S. Kim, Y. Shin, K. Hwang, J. Rim, W. Lee, H. Kim, S. Whang, J. Sue, H. Cho</i>	
Failure Analysis Of Latent Damage In Low Temperature Poly-Silicon TFT For OLED Applications	220
<i>D. Kim, C. Lim, S. Jung, D. Oh, H. Kim, W. Ho, J. Jung, J. Shim, T. Kim, K. Suh</i>	
Copper Oxidation Study by TEM	224
<i>S. Esa, R. Yahya, A. Hassan, G. Omar</i>	
Application of Seebeck Effect Imaging on Failure Analysis of Via Defect	229
<i>N. Nordin</i>	
The Auger Chemical State Analysis on Leadframe Surface Contamination	233
<i>N. Zakaria</i>	
Characterization of Si Nanowires-Based Piezoresistive Pressure Sensor by Dynamic Cycling Test	237
<i>L. Lou, H. Yan, C. He, W. Park, D. Kwong, C. Lee</i>	
Improving Yield Learning By Rapid Electrical Fault Inspection And Localization	241
<i>B. Kim, J. Hong, Y. Han, I. Kapilevich, J. Block, T. Lundquist, M. Kim</i>	
Comparison of Failure Mechanisms of ESD GGNFET Subjected to VFTLP Robustness and Reliability Tests	246
<i>W. Lai, C. Koh, B. Khoo, Y. Chen, S. Chow</i>	
Signal Propagation Analysis By Digital Lock-In Time Resolved Imaging	252
<i>G. Bascoul, P. Perdu, D. Lewis</i>	
Electrical Diagnosis of Temperature-Dependent Global Clock Failures using Probeless Isolation and Pattern Commonality Analysis	257
<i>Y. Jing, C. Meng, M. Reyes, J. Yang, P. Salinas, G. Tan</i>	
Anomalous Single Bit Retention Induced by Asymmetric STI-Corner-Thinning for Floating Gate Flash Memories	263
<i>M. Lee, W. Hsiao, R. Chen, L. Kuo, S. Dai, R. Ting, C. Chen, D. Chu, C. Lu</i>	
Developing Functional Prototypes by Package Modification Using Plasma FIB Technology	268
<i>M. Gonzales, R. Cruz, M. Parley, J. Lau, M. DiBattista, B. Routh Jr., T. Landin, P. Carleson</i>	
Reliability of Circuits Under Pads for Au and Cu Wire Bonding	273
<i>J. Gambino, J. Malinowski, A. Cote, B. Guthrie, P. Chapman, A. Vize, W. Bowe, C. Griffin, E. Cooney, T. Aoki, Y. Chen, D. Wang, M. Jaffe</i>	
Phase and Microstructure Analysis by Electron Diffraction in Semiconductor Failure Analysis	279
<i>B. Liu, Z. Mo, Q. Lei, S. Seah, C. Ye, L. Li, C. Chen, K. Chong</i>	
Capacitor Dendrite Failure Analysis for Lidless CPU Testing	283
<i>W. Huang, C. Yu, C. Cui, D. Zuo, H. Guo, C. Xie, M. Anani</i>	
Local Current Measurements for Avalanche Breakdown in Silicon p-n Junctions	287
<i>Y. Ding, D. Poenaru, D. Isakov</i>	
Impact of Field Enhancement on TDDB Lifetimes of Cu/Low-k Test Structures	293
<i>R. Ong, T. Tan, C. Gan</i>	
An Effective Broken Scan Chain Diagnosis Flow Combining Software And Hardware Solutions For Systematic Failures	298
<i>S. Goh, G. You, B. Yeoh, Y. Chan, C. Tey, C. Yap, T. Lim, T. Fei, T. Herrmann, H. Ho, R. He</i>	
Sideways FIB TEM Sample Preparation for Improved Construction Analysis in TEM	303
<i>H. Chong, B. Leer, V. Narang, M. Ho</i>	
Study of Underfill-to-Soldermask Delamination in Flip-chip Packages	307
<i>Z. Oh, R. Newman, M. Ong, F. Foo</i>	
A Simple Solution for Low-Driving-Current Output Buffer Failed at The Low Voltage ESD Zapping Event	313
<i>J. Lee, J. Shih, D. Yang, H. Kuan</i>	
Failure Analysis on Multilayer Ceramic Capacitor (MLCC) with Leakage Failure Caused by Silver (Ag) Migration in Molded Plastic Package	318
<i>K. Ng, M. Rajaratnam</i>	
Real Time Identification of Contaminants in Assembly and Test	324
<i>C. Basilio</i>	
The Link between NBTI and TDDB of High-k Gate P-MOSFETs	328
<i>Y. Gao, D. Ang</i>	

1/f Noise Measurement and Its Doping Dependencies of Si Hall Sensors	332
<i>K. Sun, M. Wang</i>	
Nanoscale Physical Analysis of Localized Breakdown Events in HfO₂/SiO_X Dielectric Stacks: A Correlation Study of STM Induced BD with C-AFM and TEM	336
<i>K. Shubhakar, K. Pey, M. Bosman, R. Thamankar, S. Kushvaha, Y. Loke, Z. Wang, N. Raghavan, X. Wu, S. O'Shea</i>	
Impact of Gate Oxide Thickness Variations on Hot-Carrier Degradation.....	343
<i>S. Tyaginov, I. Starkov, O. Triebel, M. Karner, C. Kernstock, C. Jungemann, H. Enichlmair, J. Park, T. Grasser</i>	
Charge-Pumping Extraction Techniques for Hot-Carrier Induced Interface and Oxide Trap Spatial Distributions in MOSFETs	348
<i>I. Starkov, H. Enichlmair, S. Tyaginov, T. Grasser</i>	
Comparison Of Three Methods To Measure The Internal Pressure Of Empty MEMS Packages.....	354
<i>B. Wang, S. Tanaka, J. Coster, S. Severi, A. Witvrouw, M. Wevers, I. Wolf</i>	
Outgassing Study of Thin Films Used for poly-SiGe Based Vacuum Packaging of MEMS.....	358
<i>B. Wang, S. Tanaka, B. Guo, G. Vereecke, S. Severi, A. Witvrouw, M. Wevers, I. Wolf</i>	
Advanced Scan Chain Failure Analysis Using Laser Modulation Mapping and Continuous Wave Probing	359
<i>S. Kasapi, W. Lo, J. Liao, B. Cory, H. Marks</i>	
Quantitative Aspects of Optical IC Debug Using State-of-the-Art Backside Preparation	360
<i>C. Boit, A. Glowacki, C. Pagano, U. Kerst, Y. Yokoyama</i>	
Fault Isolation Challenges and Opportunities for Proximal-Probe Imaging.....	366
<i>D. Vallett</i>	
Identification of Electrically Active Non-Visual Defects in Advanced Devices.....	372
<i>G. Bersuker</i>	
Impact of Pre-Existing Voids on Electromigration in Copper Interconnects.....	373
<i>H. Mario, M. Lim, C. Gan</i>	
The Correlation of Performance in CdTe Photovoltaics with Grain Boundaries	378
<i>M. Nowell, S. Wright, M. Scarpulla, A. Compaan, X. Liuc, N. Paudel, K. Wieland</i>	
Reliability Concerns In Copper TSV's: Methods And Results.....	385
<i>K. Croes, V. Cherman, Y. Li, L. Zhao, Y. Barbarin, J. Messemaeker, Y. Civale, D. Velenis, M. Stucchi, T. Kauerauf, A. Redolfi, B. Dimcic, A. Ivankovic, G. Plas, I. Wolf, G. Beyer, B. Swinnen, Z. Tokei, E. Beyne</i>	
Novel Electrostatic Discharge (ESD) Protection Solution in GaAs pHEMT Technology.....	390
<i>J. Liou, Q. Cui</i>	
Ultrafast Submicron Thermal Characterization of Integrated Circuits	394
<i>A. Shakouri, K. Maize, P. Jackson, X. Wang, B. Vermeersch, K. Yazawa</i>	
Advanced SEM/SPM Microscopy	396
<i>R. Heiderhoff</i>	
Dynamic Degradation Mechanisms of Low Temperature Polycrystalline Silicon Thin-Film Transistors.....	400
<i>M. Wang, H. Wang, M. Zhang, X. Lu</i>	
3D FinFET and other sub-22nm Transistors	405
<i>C. Hu</i>	
Author Index	