Technical Program

Keynote 1: Michael J. Flynn  Dataflow Supercomputing  (page 1)


Keynote 3: Deshanand Singh  Compiling OpenCL to FPGAs  (page 5)

Keynote 4: Steve Teig  Going beyond the FPGA with Spacetime

Plenary: Espen Tallaksen  FPGA development in Norwegian Industry

Side-Channel Security

Session chair: Lionel Torres

14  Detecting Power Attacks on Reconfigurable Hardware
    Adrien Le Masle and Wayne Luk

20  Efficient and Side-Channel-Secure Block Cipher Implementation with Custom Instructions on FPGA
    Suvarna Mane, Mostafa Taha and Patrick Schaumont

Software-Defined Radio

Session chair: Lesley Shannon

26  CRUSH: Cognitive Radio Universal Software Hardware
    George Eichinger, Miriam Leeser and Kaushik Chowdhury

33  Data Coding Functions for Software Defined Radios Implemented on R3TOS
    Raúl Torrego, Iñaki Val, Eñaut Muxika, Xabier Iturbe and Khaled Benkrid

Rapid Prototyping

Session chair: Ron Sass

41  EmPower: FPGA Based Rapid Prototyping of Dynamic Power Management Algorithms for Multi-Processor Systems on Chip
    Chirag Ravishankar, Sundaram Ananthanarayan, Siddharth Garg and Andrew Kennings
Limitations of Incremental Signal-Tracing for FPGA Debug
Eddie Hung and Steven J. E. Wilton

Secure Reconfiguration
Session chair: Nele Mentens

SecURe DPR: Secure Update Preventing Replay Attacks for Dynamic Partial Reconfiguration
Florian Devic, Lionel Torres, Jérémie Crenne, Benoît Badrignans and Pascal Benoît

FPGAs for Trusted Cloud Computing
Ken Eguro and Ramarathnam Venkatesan

Software-Defined Radio
Session chair: Christian Hochberger

Using DSP Block Pre-Adders in Pipeline SDF FFT Implementations in Contemporary FPGAs
Carl Ingemarsson, Petter Källström and Oscar Gustafsson

Efficient DVB-T2 Decoding Accelerator Design by Time-Multiplexing FPGA Resources
Michael Feilen, Matthias Ihmig, Christian Schwarzbauer and Walter Stechele

FPGA Routing
Session chair: Steve Wilton

On the Difficulty of Pin-to-Wire Routing in FPGAs
Niyati Shah and Jonathan Rose

Routing Algorithms for FPGAs with Sparse Intra-Cluster Routing Crossbars
Yehdhih Ould Mohammed Moctar, Guy G. F. Lemieux and Philip Brisk

Bio-inspired Applications
Session chair: Kyrre Glette

Parallel FPGA-Based All Pairs Shortest Paths for Sparse Networks: A Human Brain Connectome Case Study
Brahim Betkaoui, Yu Wang, David B. Thomas and Wayne Luk

Bio-Inspired Walking: a FPGA Multicore System for a Legged Robot
Michael Henrey, Sean Edmond, Lesley Shannon and Carlo Menon

A Scalable FPGA-Based Design for Field Programmable Large-Scale Ion Channel Simulations
Graeme Coapes, Terrence Mak, Jun Wen Luo, Alex Yakovlev and Chi-Sang Poon

Fluid Flow Simulation
Session chair: Yoshiki Yamaguchi

Scalability Analysis of Tightly-Coupled FPGA-Cluster for Lattice Boltzmann Computation
Yoshiaki Kono, Kentaro Sano and Satoru Yamamoto
FPGA Based Acceleration of Computational Fluid Flow Simulation on Unstructured Mesh Geometry
Zoltán Nagy, Csaba Nemes, Antal Hiba, András Kiss, Árpád Csík and Péter Szolgay

Reconfigurable Out-of-Order Mechanism Generator for Unstructured Grid Computation in Computational Fluid Dynamics
Takayuki Akamine, Kenta Inakagata, Yasunori Osana, Naoyuki Fujita and Hideharu Amano

Floorplanning and Placement
Session chair: Marco Platzner

Analytical Placement for Heterogeneous FPGAs
Marcel Gort and Jason H. Anderson

Profiling FPGA Floor-Planning Effects on Timing Closure
Jaren Lamprecht and Brad Hutchings

Multi-Kernel Floorplanning for Enhanced CGRAS
Aaron Wood, Adam Knight, Benjamin Ylvisaker and Scott Hauck

Applications Using PR
Session chair: Dirk Stroobandt

Optimising Explicit Finite Difference Option Pricing for Dynamic Constant Reconfiguration
Qiwei Jin, Tobias Becker, Wayne Luk and David Thomas

Exploiting Run-Time Reconfiguration in Stencil Computation
Xinyu Niu, Qiwei Jin, Wayne Luk, Qiang Liu and Oliver Pell

High-Level Design
Session chair: Joao Cardoso

A Two Step Hardware Design Method Using Clash
Rinse Wester, Christiaan Baaij and Jan Kuper

Convey Vector Personalities – FPGA Acceleration with an OpenMP-Like Programming Effort?
Björn Meyer, Jörn Schumacher, Christian Plessl and Jens Förstner

CAD Tools
Session chair: Jonathan Rose

Improving Memory Support in the VTR Flow
Andrew Somerville and Kenneth B. Kent

Verification of Streaming Designs by Combining Symbolic Simulation and Equivalence Checking
Tim Todman and Wayne Luk

Application Acceleration 1
Session chair: Stefan Wildermann
209  **Hardware Implementation of MRF MAP Inference on an FPGA Platform**  
*Jungwook Choi and Rob A. Rutenbar*

217  **CAAD BLASTP 2.0: NCBI BLASTP Accelerated with Pipelined Filters**  
*Atabak Mahram and Martin C. Herbordt*

224  **Multi Cores on FPGAs**  
*Session chair: Christian Plessl*

224  **PolyBlaze: From One to Many. Bringing the Microblaze Into the Multicore Era with Linux SMP Support**  
*Eric Matthews, Lesley Shannon and Alexandra Fedorova*

231  **Automating the Design of MLUT MPSoPC FPGAs in the Cloud**  
*David Andrews, Miaozing Huang, Azad Fakhari, Eugene Cartwright, Sen Ma, Christina Smith and Jason Agron*

237  **Application Acceleration 2**  
*Session chair: Dionisios Pnevmatikatos*

237  **A Scalable Complex Event Processing Framework for Combination of SQL-Based Continuous Queries and C/C++ Functions**  
*Takashi Takenaka, Masamichi Takagi and Hiroaki Inoue*

243  **Hardware Implementation of Motion Blur Removal**  
*Thusitha N. Chandrapala, Amila P. Cabral, Thilina S. Ambagahawaththa, Sapumal Ahangama and Jayathu G. Samarawickrama*

249  **Floating Point Arithmetic**  
*Session chair: Miriam Leeser*

249  **Correctly Rounded Floating-Point Division for DSP-Enabled FPGAs**  
*Bogdan Pasca*

255  **Reduced Complexity Single and Multiple Constant Multiplication in Floating Point Precision**  
*Martin Kumm, Katharina Liebisch and Peter Zipf*

262  **Communications and Networking**  
*Session chair: Kyle Rupnow*

262  **FPGA-Based Design and Implementation of a Multi-Gbps LDPC Decoder**  
*Alexios Balatsoukas-Stimming and Apostolos Dollas*

270  **Optimizing Packet Lookup in Time and Space on FPGA**  
*Thilan Ganegedara, Viktor Prasanna and Gordon Brebner*

277  **Architecture and FPGA Implementation of a 10.7 Gbit/s OTN Regenerator for Optical Communication Systems**
Reliability and Fault-Tolerance

Session chair: Peter Cheung

High-Level Aging Estimation for FPGA-Mapped Designs
Abdulazim Amouri and Mehdi Tahoori

Tolerating Multiple Faults with Proximate Manifestations in FPGA-Based Critical Designs for Harsh Environments
Jaime Espinosa, David de Andrés, Juan Carlos Ruiz and Pedro Gil

Overhead and Reliability Analysis of Algorithm-Based Fault Tolerance in FPGA Systems
Adam Jacobs, Grzegorz Cieslewski and Alan D. George

CAD for Partial Reconfiguration

Session chair: Suhaib Fahmy

Automatically Exploiting Regularity in Applications to Reduce Reconfiguration Memory Requirements
Fatma Abouelella, Karel Bruneel and Dirk Stroobandt

Mapping Logic to Reconfigurable FPGA Routing
Karel Heyse, Karel Bruneel and Dirk Stroobandt

Maximizing the Reuse of Routing Resources in a Reconfiguration-Aware Connection Router
Elias Vansteenkiste, Karel Bruneel and Dirk Stroobandt

Feature extraction and Classification

Session chair: David Andrews

Random Decision Tree Body Part Recognition Using FPGAs
Jason Oberg, Ken Eguro, Ray Bittner and Alessandro Forin

Acceleration of Distance-to-Default with Hardware-Software Co-Design
Izaan Allugundu, Pranay Puranik, Yat Piu Lo and Akash Kumar

An Efficient Hardware Architecture of the Optimised SIFT Descriptor Generation
Wenjuan Deng, Yiqun Zhu, Hao Feng and Zhiguo Jiang

Reconfigurable Architectures

Session chair: Brad Hutchings Brigham Young University

Adding Dataflow-Driven Execution Control to a Coarse-Grained Reconfigurable Array
Robin Panda, Carl Ebeling and Scott Hauck

A 16-Configuration-Context Robust Optically Reconfigurable Gate Array with a Reconfiguration Speed Adjustment Function
Takashi Yoza and Minoru Watanabe
<table>
<thead>
<tr>
<th>Page</th>
<th>Title</th>
<th>Authors</th>
<th>Session chair</th>
</tr>
</thead>
<tbody>
<tr>
<td>367</td>
<td>Non-Volatile 3D Stacking RRAM-Based FPGA</td>
<td>Yi-Chung Chen, Wenhua Wang, Hai Li and Wei Zhang</td>
<td></td>
</tr>
<tr>
<td>373</td>
<td>Physical Parameters Sensing</td>
<td></td>
<td>Katherine Compton</td>
</tr>
<tr>
<td>373</td>
<td>Intra-Chip Physical Parameter Sensor for FPGAs Using Flip-Flop Metastability</td>
<td>Ghaith Tarawneh, Terrence Mak and Alex Yakovlev</td>
<td></td>
</tr>
<tr>
<td>380</td>
<td>A Novel Microprocessor-Intrinsic Physical Unclonable Function</td>
<td>Abhranil Maiti and Patrick Schaumont</td>
<td></td>
</tr>
<tr>
<td>388</td>
<td>FPGA Based Key Generation Technique for Anti-Counterfeiting Methods Using Physically Unclonable Functions and Artificial Intelligence</td>
<td>Swetha Pappala, Mohammed Niamat and Weiqing Sun</td>
<td></td>
</tr>
<tr>
<td>N/A</td>
<td>On-FPGA Communication</td>
<td></td>
<td>Paul Chow</td>
</tr>
<tr>
<td>N/A</td>
<td>DESA: Distributed Elastic Switch Architecture for Efficient Networks-on-FPGAs</td>
<td>Antoni Roca, Jose Flich and Giorgos Dimitrakopoulos</td>
<td></td>
</tr>
<tr>
<td>N/A</td>
<td>An Area-Efficient Partially Reconfigurable Crossbar Switch with Low Reconfiguration Delay</td>
<td>Chin Hau Hoo and Akash Kumar</td>
<td></td>
</tr>
<tr>
<td>N/A</td>
<td>Computer Vision 1</td>
<td></td>
<td>Kentaro Sano</td>
</tr>
<tr>
<td>N/A</td>
<td>An Acceleration of a Graph Cut Segmentation With FPGA</td>
<td>Daichi Kobori and Tsutomu Maruyama</td>
<td></td>
</tr>
<tr>
<td>414</td>
<td>An FPGA Acceleration of a Level Set Segmentation Method</td>
<td>Haruhisa Tsuyama and Tsutomu Maruyama</td>
<td></td>
</tr>
<tr>
<td>421</td>
<td>IP cores and IP integration</td>
<td></td>
<td>Andreas Koch</td>
</tr>
<tr>
<td>421</td>
<td>A High Performance, Open Source SATA2 Core</td>
<td>Ashwin A. Mendon, Bin Huang and Ron Sass</td>
<td></td>
</tr>
<tr>
<td>429</td>
<td>IP-XACT Extensions for IP Interoperability Guarantees and Software Model Generation</td>
<td>Thomas P. Perry, Richard L. Walke, Rob Payne, Stefan Petko and Khaled Benkrid</td>
<td></td>
</tr>
<tr>
<td>437</td>
<td>Application Acceleration 3</td>
<td></td>
<td>Koen Bertels</td>
</tr>
<tr>
<td>437</td>
<td>K-Means Implementation on FPGA for High-Dimensional Data Using Triangle Inequality</td>
<td>Zhongduo Lin, Charles Lo and Paul Chow</td>
<td></td>
</tr>
</tbody>
</table>
Enhancing Performance of Tall-Skinny QR factorization Using FPGAs
Abid Raque, Nachiket Kapre and George A. Constantinides

Computer Vision
Session chair: Apostolos Dollas

Real-Time Corner and Polygon Detection System on FPGA
Chunmeng Bi and Tsutomu Maruyama

Deep-Pipelined FPGA Implementation of Ellipse Estimation for Eye Tracking
Keisuke Dohi, Yuma Hatanaka, Kazuhiro Negi, Yuichiro Shibata and Kiyoshi Oguri

Cryptography
Session chair: Jason Anderson

A Benign Hardware Trojan on FPGA-Based Embedded Systems
Jason X. Zheng, Ethan Chen and Miodrag Potkonjak

Breaking the GSM A5/1 Cryptography Algorithm with Rainbow Tables and High-End FPGAs
Maria Kalenderi, Dionisios Pnevmatikatos, Ioannis Papaefstathiou and Charalampos Manifavas

PHD Forum (Wednesday)

A Resiliency-Aware Scheduling Approach for FPGA Configuration: Preliminary Results
Jeremy Abramson and Pedro C. Diniz

Power/Performance Optimization in FPGA-Based Asymmetric Multi-Core Systems
Bruno De Abreu Silva and Vanderlei Bonato

Thermal-Aware Partitioning for 3D FPGAs
Krishna Chaitanya Nunna, Farhad Mehdipour and Kazuaki Murakami

Reconfigurable Multi-Processor Architecture For Streaming Applications
Leyla S. Ghazanfari, Roberto Airoldi, Jari Nurmi and Tapani Ahonen

NoC-AXI Interface for FPGA-based MPSoc Platforms
Marco Ramirez, Masoud Daneshtalab, Juha Plosila and Pasi Liljeberg

Modeling of Dynamic Reconfigurable Systems with Haskell
Bahram N. Uchevler and Kjetil Svarstad

Stimulation Board for Automated Verification of Touchscreen-based Devices
Ivan Kastelan, Vladimir Marinkovic, Radomir Dzakula, Nikola Vranic and Vukota Pekovic

High Level Structural Description of Streaming Applications
Anja Niedermeier, Jan Kuper and Gerard J.M. Smit
Ambient Hardware and the Case for Transcoding Media Streams
Milica Orlandi and Kjetil Svarstad

Combining Data and Computation Transformations for Fine-Grain Reconfigurable Architectures
Cristiano B. Oliveira and Eduardo Marques

Implementation ans Outcomes of FPGA-based System Design in Mongolian Education
D. Erdenechimeg, Ts. Sugir Computer Engineering Department CSMS - MUST, Mongolia
F. Philipp and M. Glesner Microelectronic Systems Research Group, TU Darmstadt, Germany

Poster Session 1

CaaS: Core as a Service Realizing Hardware Services on Reconfigurable MPSoCs
Chao Wang, Xi Li, Junneng Zhang, Peng Chen and Xuehai Zhou

Hardware Acceleration and Data-Utility Improvement for Low-Latency Privacy Preserving Mechanism
Junichi Sawada and Hiroaki Nishi

Dataflow Graph Partitioning for High Level Synthesis
Sharad Sinha and Thambipillai Srikanthan

A Fast and High Quality Stereo Matching Algorithm on FPGA
Minxi Jin and Tsutomu Maruyama

An FPGA Aligner for Short Read Mapping
Yupeng Chen, Bertil Schmidt and Douglas L. Maksell

Raising the Abstraction Level of HDL for Control-Dominant Applications
Marc-Andre Daigneault and Jean Pierre David

A Two-Stage Variation-Aware Placement Method for FPGAs Exploiting Variation Maps Classification
Zhenyu Guan, Justin S. J. Wong, Sumanta Chaudhuri, George Constantinides and Peter Y. K. Cheung

Speedy Bus Mastering PCI Express
Ray Bittner

Adaptive Sequential Monte Carlo Approach for Real-Time Applications
Thomas C.P. Chau, Wayne Luk, Peter Y.K. Cheung, Alison Eele and Jan Maciejowski

From OpenCL to High-Performance Hardware on FPGAs
Tomasz S. Czajkowski, Utku Aydonat, Dmitry Denisenko, John Freeman, Michael Kinsner, David Neto, Jason Wong, Peter Yiannacouras and Deshanand
A Framework for Open Tiled Manycore System-on-Chip
Stefan Wallentowitz, Andreas Lankes, Aurang Zaib, Thomas Wild and Andreas Herkersdorf

Fault Detection and Avoidance of FPGA in Various Granularities
Kazuki Inoue, Yuki Nishitani, Motoki Amagasaki, Masahiro Iida, Morihiro Kuga and Toshinori Sueyoshi

CMA-Cube: a Scalable Reconfigurable Accelerator with 3-D Wireless Inductive Coupling Interconnect
Yusuke Koizumi, Eiichi Sasaki, Hideharu Amano, Hiroki Matsutani, Yasuhiro Take, Tadahiro Kuroda, Ryuichi Sakamoto, Mitaro Namiki, Kimiyoshi Usami, Masaaki Kondo, and Hiroshi Nakamura

Implementation Techniques for Evolvable HW Systems: Virtual vs. Dynamic Reconfiguration
Ruben Salvador, Andres Otero, Javier Mora, Eduardo de la Torre, Teresa Riesgo and Lukáš Sekanina

Development of an FPGA-based Real-Time P300 Speller
Kanav Khurana, Pooja Gupta, Rajesh C. Panicker and Akash Kumar

Influence of Operating Conditions on Ring Oscillator-Based Entropy Sources in FPGAs
Christian Hochberger, Changgong Li, Michael Raitza and Markus Vogt

Exploration of Ring Oscillator Design Space for Temperature Measurements on FPGAs
Christoph Ruething, Andreas Agne, Markus Happe and Christian Plessl

Extending BORPH for Shared Memory Reconfigurable Computers
Xun Changqing, Wen Mei, Wu Nan, Zhang Chunyuan and Hayden Kwok-Hay So

Automatic Generation of Application-Specific Accelerators for FPGAs from Python Loop Nests
David Shefeld, Michael Anderson and Kurt Keutzer

PPMC: Hardware Scheduling and Memory Management Support for Multi Accelerators
Tassadaq Hussain, Miguel Pericàs, Nacho Navarro and Eduard Ayguadé

Performance Analysis of Fully-Adaptable CRC Accelerators on an FPGA
Amila Akagic and Hideharu Amano

Dynamic Multiobjective Optimization Management of the Energy-Performance-Accuracy Space for Separable 2-D Complex Filters
Daniel Llamocca, Cesar Carranza and Marios Pattichis

HCM: An Abstraction Layer for Seamless Programming of DPR FPGA
Yan Xu, Olivier Muller, Pierre-Henri Horrein and Frédéric Pétrot
587 Early Performance Estimation of Image Compression Methods on Soft Processors
Adam Powell, Christos-S. Bouganis and Peter Y.K. Cheung

Area Estimation of Look-Up Table Based Fixed-Point Computations on the Example of a Real-Time High Dynamic Range Imaging System
Michael Kunz, Martin Kumm, Martin Heide and Peter Zipf

595 Sliding Block Viterbi Decoders in FPGA
Mário Véstias, Horácio Neto and Helena Sarmento

599 Dynamic Query Switching for Complex Event Processing on FPGAs
Masamichi Takagi, Takashi Takenaka and Hiroaki Inoue

603 Dual-Core Motion Estimation Processor
Joaquín Olivares and José M. Palomares

On the Automatic Integration of Hardware Accelerators into FPGA-Based Embedded Systems
Christian Pilato, Andrea Cazzaniga, Gianluca Durelli, Andres Otero, Donatella Sciuto and Marco D. Santambrogio

611 Design of a Novel Quantum-Dot Cellular Automata Field Programmable Gate Array
Hemant Balijepalli and Mohammed Niamat

A Predictive Delay Fault Avoidance Scheme for Coarse-Grained Reconfigurable Architecture
Toshihiro Kameda, Hiroaki Konoura, Dawood Alnajjar, Yukio Mitsuyama, Masanori Hashimoto and Takao Onoye

615 DWARV 2.0: A CoSy-based C-to-VHDL Hardware Compiler
Razvan Nane, Vlad-Mihai Sima, Bryan Olivier, Roel Meeuws, Yana Yankova and Koen Bertels

623 Low Area Memory-Free FPGA Implementation of the AES Algorithm
Junfeng Chu and Mohammed Benaissa

An Adaptive FPGA Implementation of Multi-Core K-Nearest Neighbour Ensemble Classifier Using Dynamic Partial Reconfiguration
Hanaa Hussain, Khaled Benkrid, Chuan Hong and Huseyin Seker

631 Fast Digital Rendering for Special Effects
Sam Collinson and John Morris

635 Design and Utilization of an FPGA Cluster to Implement a Digital Wireless Channel Emulator
Scott Buscemi and Ron Sass

639 Wire-Speed Verification Schemes for HW/SW Design of 10-Gbit/s-Class Large-Scale NW SoC Using Multiple FPGAs
Kazuhiko Terada, Hiroyuki Uzawa, Namiko Ikeda, Satoshi Shigematsu, Nobuyuki Tanaka and Masami Urano
<table>
<thead>
<tr>
<th>Page</th>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>643</td>
<td>A New Self-Adapting Architecture for Feature Detection</td>
<td>Paulo Da Cunha Possa, Sidi Ahmed Mahmoudi, Naim Harb and Carlos Valderrama</td>
</tr>
<tr>
<td>647</td>
<td>Custom Instructions with Local Memory Elements Without Expensive DMA Transfers</td>
<td>Alok Prakash, Christopher T. Clarke and Thambipillai Srikanthan</td>
</tr>
<tr>
<td>651</td>
<td>Dual MicroBlaze Rekeying Processor for Group Key Management</td>
<td>José M. Granado-Criado, Miguel A. Vega-Rodriguez, Juan M. Sanchez-Perez and Juan A. Gomez-Pulido</td>
</tr>
<tr>
<td>655</td>
<td>Lightweight Reconfiguration Security Services for AXI-Based MPSoCs</td>
<td>Pascal Cotret, Guy Gogniat, Jean-Philippe Diguet and Jérémie Crenne</td>
</tr>
<tr>
<td>659</td>
<td>Examination of the Concept of a Row-Column Separated Median Filter</td>
<td>D. Wang, C. T. Clarke and A. N. Evans</td>
</tr>
<tr>
<td>663</td>
<td>On Reconfigurable Fabrics and Generic Side-Channel Countermeasures</td>
<td>Rob Beat, Philipp Grabher, Dan Page, Stafan Tillich and Marcin Wójcik</td>
</tr>
<tr>
<td>667</td>
<td>Hardware Implementation of Stereo Correspondence Algorithm for the ExoMars Mission</td>
<td>G. Lentaris, D. Diamantopoulos, K. Siozios, D. Soudris and M. Avilés Rodríguez</td>
</tr>
<tr>
<td>671</td>
<td>Design Space Exploration for Automatically Generated Cryptographic Hardware Using Functional Languages</td>
<td>Davy Wolfs, Kris Aerts and Nele Mentens</td>
</tr>
<tr>
<td>675</td>
<td>Fast and Accurate Single Bit Error Injection into SRAM Based FPGAs</td>
<td>U. Kretzschmar, A. Astarloa, J. Jiménez, M. Garay and J. Del Ser</td>
</tr>
<tr>
<td>679</td>
<td>(GECO)&lt;sup&gt;2&lt;/sup&gt;: A Graphical Tool for the Generation of Configuration Bitstreams for a Smart Sensor Interface Based on a Coarse-Grained Dynamically Reconfigurable Architecture</td>
<td>François Philipp and Manfred Glesner</td>
</tr>
<tr>
<td>683</td>
<td>Design and Implementation of Fault-Tolerant Soft Processors on FPGAs</td>
<td>Chuan Hong, Khaled Benkrid, Xabier Iturbe and Ali Ebrahim</td>
</tr>
<tr>
<td>687</td>
<td>Towards GCC-Based Automatic Soft-Core Customization</td>
<td>Gerald Hempel, Christian Hochberger and Michael Raitza</td>
</tr>
<tr>
<td>691</td>
<td>An Energy-Efficient Hardware Accelerator for Robust Header Compression in LTE-Advanced Terminals</td>
<td>Shadi Traboulsi, Wenlong Zhang, Daivd Szczesny, Anas Showk and Attila Bilgic</td>
</tr>
<tr>
<td>695</td>
<td>Exploring the Latency-Resource Trade-off for the Discrete Fourier Transform on the FPGA</td>
<td>Gordon Inggs, David Thomas and Simon Winberg</td>
</tr>
<tr>
<td>699</td>
<td>iTester: A FPGA Based High Performance Traffic Replay Tool</td>
<td></td>
</tr>
</tbody>
</table>
Fuxing Zhang, Yingke Xie, Junjie Liu, Layong Luo, Qingsong Ning and Xiaolong Wu

Modeling and Synthesis of a Dynamic and Partial Reconfiguration Controller
S. Guillet, F. de Lamotte, N. Le Griguer, È Rutten, J.-P. Diguet, G. Gogniat

An Open-Source Design and Validation Platform for Reconfigurable Systems
Alessandra Bonetto, Andrea Cazzaniga, Gianluca Durelli, Christian Pilato, Donatella Sciuto and Marco D. Santambrogio

Floating Point HOG Implementation for Real-Time Multiple Object Detection
Mateusz Komorkiewicz, Maciej Kluczewski and Marek Gorgon

Runtime Reconfigurable DSP Unit Using One's Complement and Minimum Signed Digit
Travis Manderson and Laurence Turner

A High Performance and Low Energy Intra Prediction Hardware for High Efficiency Video Coding
Ercan Kalali, Yusuf Adibelli and Ilker Hamzaoglu

High-Level Linear Projection Circuit Design Optimization Framework for FPGAs Under Over-Clocking
Rui Policarpo Duarte and Christos-Savvas Bouganis

Evaluating the Efficiency of DSP Block Synthesis Inference from Flow Graphs
Bajaj Ronak and Suhaib A. Fahmy

System#: High-Level Synthesis of Physical Simulations for FPGA-Based Real-Time Execution
Christian Köllner, Nico Adler and Klaus Müller-Glaser

BIL: A Tool-Chain for Bitstream Reverse-Engineering
Florian Benz, André Seffrin and Sorin A. Huss

A Region Merging Approach for Image Segmentation on FPGA
Dang Ba Khac Trieu and Tsutomu Maruyama

On Measurement of Impact of the Metallization and FPGA Design to the Changes of Slice Parameters and Generation of Delay Faults
Petr Pfeifer and Zdenek Pliva