2012 IEEE International SOC Conference

(SOCC 2012)

Niagara Falls, New York, USA
12 – 14 September 2012
# TABLE OF CONTENTS

Keynote: Driving Innovation in the "Post-Silicon" World

Bernard S. Meyerson, IBM Fellow, Vice President, Innovation & Global University Relations IBM Systems and Technology Group

Session PL1: Plenary Session

*Chair: Norbert Schuhmann, Fraunhofer Institute for Integrated Circuits - IIS, Germany*

- **PL1.1 “Low Power Solutions for a Smarter Future”**
  Richard Grisenthwaite, ARM Fellow, VP of Technology, ARM

- **PL1.2 "Era of SoCs: Challenges and Opportunities”**
  Raj Yavatkar, Intel Fellow, Director, System-on-Chip Architecture, Intel Corporation

Session WPA1: Green Circuits & Design Methodologies

*Chair: Kenneth Hsu, Rochester Institute of Technology, Rochester, NY*

- **WPA1.1 An Energy-Efficient Level Converter with High Thermal Variation Immunity for Sub-threshold to Super-threshold Operation**
  Mei-Wei Chen, Ming-Hung Chang, Wei Hwan
  National Chiao Tung University, Taiwan

- **WPA1.2 An On-Chip 250 mA 40 nm CMOS Digital LDO Using Dynamic Sampling Clock Frequency Scaling with Offset-Free TDC-Based Voltage Sensor**
  Kazuo Otsuga
  Renesas Electronics Corporation, Japan

- **WPA1.3 A BETTER-THAN-WORST-CASE CIRCUIT DESIGN METHODOLOGY USING TIMING-ERROR SPECULATION AND FREQUENCY ADAPTATION**
  Sebastian Moreno Londoño and Jose Pineda de Gyvez
  Eindhoven University of Technology, Netherlands

- **WPA1.4 Variation-and-Aging Aware Low Power embedded SRAM for Multimedia Applications**
  Na Gong, Shixiong Jiang, Anoosha Challapalli, Manpinder Panesar, Ramalingam Sridhar
  University at Buffalo

- **WPA1.5 pbCAM: probabilistically-banked Content Addressable Memory**
  Tolga Soyata and John Liobe
Session WPB1: Analog, Mixed Signal and Biomedical Circuits

Chair: Poki Chen, National Taiwan University of Science and Technology, Taiwan

WPB1.1 ADPLL Variables Determinations based on Phase Noise, Spur and Locking Time
Bo Jiang and Tian Xia
University of Vermont

WPB1.2 A NOVEL DIGITAL LOOP FILTER ARCHITECTURE FOR BANG-BANG ADPLL
Moataz Abdelfattah¹, Amr Lotfy², Mohamed Abdelsalam², Mohamed Abdel-moneum², Nasser Kurd², Maged Ghoneima¹, Greg Taylor², Yehea Ismail¹
¹American University in Cairo, ²Intel Corporation

WPB1.3 A 1.7GS/s 6-BIT FLASH A/D CONVERTER WITH DISTRIBUTED OFFSET CANCELLING SAMPLE-ANDHOLD
Lampros Mountrichas, Theodore Laopoulos, Stylianos Siskos
Aristotle University of Thessaloniki, Greece

WPB1.4 A 1.62/2.7/5.4Gbps clock and data recovery circuit for DisplayPort 1.2
Jin-Cheol Seo, Sang-Soon Im, Kwan Yoon, Seung-Wook Oh, Taek-Joon An, Gi-Yeol Bae, Jin-Ku Kang
Inha University, South Korea

WPB1.5 Gray-level image recognition on a dynamically reconfigurable vision architecture
Yuki Kamikubo, Minoru Watanabe, Shoji Kawahito
Shizuoka University, Japan

WPB1.6 A Read-Assist, Write-Back Voltage Sense Amplifier for Low-Voltage Operated SRAMs
Tahseen Shakir and Manoj Sachdev
University of Waterloo, Canada

Session WPA2: Reconfigurable and Programmable Logic

Chair: Poki Chen, National Taiwan University of Science and Technology, Taiwan

WPA2.1 SYNTHESISABLE DELAY LINE ARCHITECTURES FOR DIGITALLY CONTROLLED VOLTAGE REGULATORS
Omar Haridy¹, Harish Krishnamurthy², Amr Helmy¹, Yehea Ismail¹
¹The American university in Cairo, Egypt, ²Intel Lab, USA

WPA2.2 A Novel Design Flow for a 3D Heterogeneous System Prototyping Platform
Chun-Ming Huang, Chih-Chyau Yang, Chien-Ming Wu, Chun-Chieh Chiu, Yi-Jun Liu, Chun-Chieh Chu, Nien-Hsiang Chang, Wen-Ching Chen, Chih-Hsing Lin, Hua-Hsin Luo
National Chip Implementation Center, Taiwan
WPA2.3 An FPGA Implementation for a High-Speed Optical Link With a PCIe Interface

Edin Kadric¹, Naraig Manjikian², Zeljko Zilic¹
¹McGill University, Canada, ²Queen's University, Canada

Session WPB2: Emerging Technologies

Chair: Thanh Tran, Texas Instruments

WPB2.1 Invited Talk: Noise and mismatch in sub 28nm silicon processes

Andrew Marshall, Texas Instruments

WPB2.2 Reconfigurable RRAM for LUT Logic Mapping: A Case Study for Reliability Enhancement

Matthew Catanzaro and Dhireesha Kudithipudi
Rochester Institute of Technology

WPB2.3 LIMITATIONS OF INTEGRATING FIELD INDUCED AGGREGATION BASED FAULT REPAIR AUTOMATONS WITH INTEGRATED CIRCUITS

Aveek Dutta and Sanjiv Sambandan
Indian Institute of Science, Bangalore, India

Session WPP: Poster & Reception

Chair: Norbert Schuhmann, Fraunhofer IIS
CoChair: Kaijian Shi, Cadence Design Systems

WPP1.1 Efficient Generation of Analog Circuit Models for Accelerated Mixed-Signal Simulation

Stefan Hoeldampf, Hyun-Sek Luk as Lee, Daniel Zaum, Mark us Olbrich, Erich Barke
Institute of Microelectronic Systems, Leibniz Universität Hannover, Germany

WPP1.2 Neural Recording System with Low-Noise Analog Front-End and Comparator-Based Cyclic ADC

Susie Kim, Seung-In Na, Tae-Hoon Kim, Hyunjoong Lee, Sunkwon Kim, Cyuyeol Rhee, Suhwan Kim
Seoul National University, South Korea

WPP1.3 Methodology to Determine Dominant Noise Source in a System-On-Chip Based Implantable Device

Zhihua Gan, Emre Salman, Milutin Stanacevic
Stony Brook University

WPP1.4 A Wide Tuning Range QCCO Based on CMOS Active Inductors

Jun Zhang and Huihua Liu
Research Institution of Electronic Science and Technology of UESTC, China

WPP1.5 Evaluation of Layout Design Styles using a Quality Design Metric

Sergio Gomez and Francesc Moll
Universitat Polit`ecnica de Catalunya, Spain


Cory Merkel, Dhireesha Kudithipudi, Andres Kwasinski
Rochester Institute of Technology
WPP1.7 Design of Near Threshold All Digital Delay Locked Loops

Mehdi Sadi and Mircea Stan
University of Virginia

WPP1.8 A stable Chip-ID Generating Physical Uncloneable Function using Random Address Errors in SRAM

Hidehiro Fujiwara, Makoto Yabuuchi, Yasumasa Tsukamoto, Hiroyumi Nakano, Toru Owada, Hiroyuki Kawai, Koji Nii
Renesas Electronics Corporation, Japan

WPP1.9 STT-MRAM Memory Cells with Enhanced On/Off Ratio

Ravi Patel, Engin Ipke, Eby Friedman
University of Rochester

WPP1.10 Efficient High-speed Current-mode Links for Network-on-Chip Performance Optimization

Hamed Sajjadikia and Cristinel Ababei
North Dakota State University

WPP1.11 Electrical and Fluidic Microbumps for 3D-IC and Silicon Interposer

Li Zheng and Muhamad Bakir
Georgia Institute of Technology

WPP1.12 INTERCONNECT COMPRESSION AND ITS BENEFITS FOR MULTI-CORE SYSTEMS

Jiangjiang Liu and Jianyong Zhang
Lamar University

WPP1.13 Ventti: a Vertically Integrated Framework for Simulation and Optimization of Networks-On-Chip

Young Jin Yoon, Nicola Concer, Luca Carloni
Columbia University

WPP1.14 Reconfigurable Framework for High-Bandwidth Stream-Oriented Data Processing

Alexander Mykyta\textsuperscript{1}, Dorin Patru\textsuperscript{1}, Eli Saber\textsuperscript{1}, Gene Roylance\textsuperscript{2}, Brad Larson\textsuperscript{2}
\textsuperscript{1}Rochester Institute of Technology, \textsuperscript{2}Hewlett-Packard

WPP1.15 A Testability-aware Low Power Architecture

Gang Wang, Jian Wang, Zi-Chu Qi
Chinese Academy of Sciences, Beijing, China

Session PL2: Plenary Talk

Chair: Kaijian Shi, Cadence Design Systems

PL2.1 Connectivity Driven Systems: On-Chip, Off-chip and In-between
Robert Geer, College of Nanoscale Science and Engineering (CNSE), University of Albany, SUNY

Session TA1: Wireline and Wireless Communication Circuits

Chair: Sao-Jie Chen, National Taiwan University, Taiwan

TA1.1 Multi-Objective Optimization of Radio-Frequency Front-Ends

192
Session TB1: Embedded Systems, Multi-Core

Chair: Yuejian Wu, Infinera, Ottawa, Canada

TB1.1 A 55nm 0.5V 128Kb Cross-Point 8T SRAM with Data-Aware Dynamic Supply Write-Assist 218

Yung-Wei Lin1, Hao-I Yang1, Mao-Chih Hsia1, Yi-Wei Lin1, Chien-Hen Chen1, Ching-Te Chuang1, Wei Hwang1, Nan-Chun Lien1, Kuen-Di Lee2, Wei-Chiang Shih2, Ya-Ping Wu2, Wen-Ta Lee2, Chih-Chiang Hsu2

1National Chiao Tung University, Taiwan 2Faraday Technology Corporation, Taiwan

TB1.2 LOW POWER 6T-SRAM WITH TREE ADDRESS DECODER USING A NEW EQUALIZER PRECHARGE SCHEME 224

YUAN REN, MICHAEL GANSEN, TOBIAS G. NOLL
RWTH Aachen University, Germany

TB1.3 Efficient, Snoopless, SoC Coherence 230

Stefanos Kaxiras1 and Alberto Ros2

1Uppsala University, Sweden, 2University of Murcia, Spain

TB1.4 SOLARCAP: Super Capacitor Buffering of Solar Energy for Self-Sustainable Field Systems 236

Amal Fahad, Tolga Soyata, Tai Wang, Gaurav Sharma, Wendi Heinzelman, Kai Shen
University of Rochester

Session TPA1: System Level Design EDA Tools

Chair: Hai (Helen) Li, Polytechnic Institute of NYU, New York, USA

TPA1.1 AN APPROACH FOR QUANTITATIVE OPTIMIZATION OF HIGHLY EFFICIENT DEDICATED CORDIC

MACROS AS SoC BUILDING BLOCKS

UPASNA VISHNOI, MICHAEL MEIXNER, TOBIAS G. NOLL
RWTH Aachen University, Germany
Session TPB1: Signal Integrity, DFT and Verification

Chair: Yuejian Wu, Infinera, Ottawa, Canada

TPB1.1 Multi-Clock DFT Architecture for Interface Characterization and Power

Chris Ryan
Maxim Integrated Products

TPB1.2 Optimal Power-Constrained SoC Test Schedules With Customizable Clock Rates

Vijay Sheshadri, Vishwani Agrawal, Prathima Agrawal
Auburn University

TPB1.3 Efficient Fault Emulation using Automatic Pre-Injection Memory Access Analysis

Johannes Grinschgl1, Armin Krieg1, Christian Steger1, Reinhold Weiss1, Holger Bock2, Josef Haid2
1 Graz University of Technology, Austria 2 Infineon Technologies Austria AG

TPB1.4 MUTATION-ANALYSIS DRIVEN FUNCTIONAL VERIFICATION OF A SOFT MICROPROCESSOR

Tao Xie1, Wolfgang Müller1, Florian Letombe2
1 University of Paderborn, Germany 2 SpringSoft Inc.

Session TPT1: Embedded Tutorial I

Chair: Nagi Naganathan, LSI Corporation

TPT1.1 Intellectual Property Protection and Security

Susmita Sur-Kolay, Indian Statistical Institute

Session TPT2: Embedded Tutorial II

Chair: Yiran Chen, University of Pittsburgh

TPT2.1 Neuromorphic Computing: A SoC Scaling Path for the Next Decade

Organizer: Yiran Chen, University of Pittsburgh
Moderator: Qing Wu, Air Force Research Laboratory
TPT2.2 Exploiting Memristive Device Behavior for Emerging Digital Logic and Memory Applications
Garrett Rose
Air Force Research laboratory

TPT2.3 Massive Parallel Neuromorphic Computing Model for Intelligent Text Recognition
Qinru Qiu
Syracuse University

TPT2.4 Memristor in Neuromorphic Computing
Hai (Helen) Li
Poly-NYU

Session FA1: Network on Chips, 3D-ICs

Chair: Danella Zhao, University of Lousiana at Lafayette

FA1.1 Power-Area Analysis of NoCs in FPGAs
Mohammadreza Binesh Marvasti and Ted. H Szymanski
McMaster University, Canada

FA1.2 DVFS-ENABLED SUSTAINABLE WIRELESS NoC ARCHITECTURE
Jacob Murray, Partha Pande, Behrooz Shirazi
Washington State University

FA1.3 Design Space Exploration for Robust Power Delivery in TSV Based 3-D Systems-on-Chip
Suhas Satheesh and Emre Salman
Stony Brook University

FA1.4 A Scalable Electrical Characterization Method for Inter-Strata Interconnects in 3-D ICs
Tian Xia\textsuperscript{1} and Guoan Wang\textsuperscript{2}
\textsuperscript{1}University of Vermont, \textsuperscript{2}University of South Carolina

Session FB1: Digital Signal Processing & Multimedia Systems

Chair: Nagi Naganathan, LSI Corporation

FB1.1 Stacking Memory Architecture Exploration for Three-Dimensional Integrated Circuit in 3-D PAC
Hsien-Ching Hsieh, Po-Han Huang, Chi-Hung Lin, Huang-Lun Lin
Industrial Technology Research Institute, Taiwan

FB1.2 Aging-Aware Reliable Multiplier Design
Yu-Hung Cho, Ing-Chao Lin, Yi-Ming Yang
National Cheng Kung University, Taiwan

FB1.3 A Digital Neuromorphic VLSI Architecture with Memristor Crossbar Synaptic Array for Machine Learning
Yongtae Kim, Yong Zhang, Peng Li
Texas A&M University
FB1.4 A Novel Flexible Foldable Systolic Architecture FIR Filters Generator

Hang Yin¹, Weitao Du¹, Yu Hen Hu², Rui Lv¹
¹Communication University of China, ²University of Wisconsin-Madison

Session FA2: Network on Chips, 3D-ICs II

Chair: Sakir Sezer, Queen’s University Belfast, UK

FA2.1 A Sensor-less NBTI mitigation methodology for NoC architectures

Davide Zoni and William Fornaciari
Politecnico di Milano, Italy

FA2.2 Design of a Scalable RF Microarchitecture for Heterogeneous MPSoCs

Danella Zhao and Yi Wang
University of Louisiana at Lafayette

FA2.3 Design of An NoC with On-chip Photonic Interconnects Using Adaptive CDMA links

Soumyajit Poddar, Prasun Ghosa, Priyajit Mukherjee, Suman Samui, Hafizur Rahaman
Bengal Engineering and Science University, Shibpur, India

FA2.4 Design of Interlock-Free Combined Allocators for Networks-on-Chip

Ye Lu¹, Changlin Chen², John McCanny¹, Sakir Sezer¹
¹Queen’s University of Belfast, ²Delft University of Technology

FA2.5 MAZENOC: Novel Approach for Fult-Tolerant NOC Routing

Eduardo Wachter and Fernando Moraes
PUCRS, Brazil

Session FB2: Design for Manufacturability, Variation aware Methodologies

Chair: Nagi Naganathan, LSI Corporation

FB2.1 ON-CHIP SELF-CALIBRATED PROCESS-TEMPERATURE SENSOR FOR TSV 3D INTEGRATION

Tzu-Ting Chiang, Po-Tsang Huang, Wei Hwang
National Chiao Tung University, Taiwan

FB2.2 Calibration of Propagation Delay of Flip-Flops

Tamer Ragheb and Andrew Marshall
Texas Instruments Inc

FB2.3 Native-Conflict-Avoiding Track Routing for Double Patterning Technology

Bi-Ting Lai, Tai-Hung Li, Tai-Chen Chen
National Central University, Taiwan

FB2.4 Variation tolerant self-adaptive clock generation architecture based on a ring oscillator

Jordi Pérez-Puigdemont, Antonio Calomarde, Francesc Moll
Universitat Politècnica de Catalunya , Spain