2013 23rd International Conference on Field Programmable Logic and Applications

(FPL 2013)

Porto, Portugal
2 – 4 September 2013
# TABLE OF CONTENTS

## Regular Papers

### Session M1A: Infrastructure, Interconnect and Communication

**Session Chair: Peter Cheung (Imperial College London, UK)**

**Automated Synthesis of FPGA-Based Heterogeneous Interconnect Topologies**  
Alessandro Cilardo, Edoardo Fusella, Luca Gallo, Antonino Mazzeo

**Generating Infrastructure for FPGA-Accelerated Applications**  
Myron King, Asif Khan, Abhinav Agarwal, Oriol Arcas, Arvind

**The Power of Communication: Energy-Efficient NoCs for FPGAs**  
Mohamed Abdelfattah, Vaughn Betz

### Session M1B: Defects, Faults, and Aging

**Session Chair: Kentaro Sano (Tohoku University, Japan)**

**Altering LUT Configuration for Wear-Out Mitigation of FPGA-Mapped Designs**  
Parthasarathy Murali Baskar Rao, Abdulazim Amouri, Saman Kiamehr, Mehdi Tahoori

**Improving Autonomous Soft-Error Tolerance of FPGA Through LUT Configuration Bit Manipulation**  
Anup Das, Shyamsundar Venkataraman, Akash Kumar

**Defect-Robust FPGA Architectures for Intellectual Property Cores in System LSI**  
Motoki Amagasaki, Kazuki Inoue, Qian Zhao, Masahiro Iida, Morihiro Kuga, Toshinori Sueyoshi

### Session M1C: Application Acceleration

**Session Chair: Oliver Diesel (University of New South Wales, Australia)**

**Accelerating Random Forest Training Process Using FPGA**  
Chuan Cheng, Christos-Savvas Bouganis

**FPGA-Based K-Means Clustering Using Tree-Based Data Structures**  
Felix Winterstein, Samuel Bayliss, George A. Constantinides

**Accelerating Maximum Likelihood Estimation for Hawkes Point Processes**  
Ce Guo, Wayne Luk

### Session M2A: FPGA Infrastructure and Design Environments

**Session Chair: Diana Göhringer (Ruhr-Universität Bochum, Germany)**

**Titan: Enabling Large and Complex Benchmarks in Academic CAD**  
Kevin E. Murray, Scott Whitty, Suya Liu, Jason Liu, Vaughn Betz

**RIFFA 2.0: A Reusable Integration Framework for FPGA Accelerators**  
Matthew Jacobsen, Ryan Kastner

**In Pursuit of Instant Gratification for FPGA Design**  
Andrew Love, Wenwei Zha, Peter Athanas

### Session M2B: Application Acceleration
<table>
<thead>
<tr>
<th>Session M2C: FPGA Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Session Chair: Leonel Sousa (Instituto Superior Técnico / INESC-ID, Portugal)</td>
</tr>
<tr>
<td><strong>Charge Recycling for Power Reduction in FPGA Interconnect</strong></td>
</tr>
<tr>
<td>Safeen Huda, Jason Anderson, Hirotaka Tamura</td>
</tr>
<tr>
<td><strong>Impact of Hard Macro Size on FPGA Clock Rate and Place/Route Time</strong></td>
</tr>
<tr>
<td>Chris Lavin, Brent Nelson, Brad Hutchings</td>
</tr>
<tr>
<td><strong>Should FPGAs Abandon the Pass-Gate?</strong></td>
</tr>
<tr>
<td>Charles Chiasson, Vaughn Betz</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Session M3A: Placement and Routing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Session Chair: Tobias Becker (Imperial College London, UK)</td>
</tr>
<tr>
<td><strong>StaticRoute: A Novel Router for the Dynamic Partial Reconfiguration of FPGAs</strong></td>
</tr>
<tr>
<td>Brahim Al Farisi, Karel Bruneel, Dirk Stroobandt</td>
</tr>
<tr>
<td><strong>Criticality-Based Routing for FPGAs with Reverse Body Bias Switch Box Architectures</strong></td>
</tr>
<tr>
<td>Wei Ting Loke, Wenfeng Zhao, Yajun Ha</td>
</tr>
<tr>
<td><strong>A Run-Time Graph-Based Polynomial Placement and Routing Algorithm for Virtual FPGAs</strong></td>
</tr>
<tr>
<td>Ricardo Ferreira, Luciana Rocha, Andre G. dos Santos, Jose A. Nacif, Stephan Wong, Luigi Carro</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Session M3B: Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Session Chair: Horácio C. Neto (IST/INESC-ID, Portugal)</td>
</tr>
<tr>
<td><strong>A High-Performance Overlay Architecture for Pipelined Execution of Data Flow Graphs</strong></td>
</tr>
<tr>
<td>Davor Capalija, Tarek Abdelrahman</td>
</tr>
<tr>
<td><strong>Efficient Implementation of Virtual Coarse Grained Reconfigurable Arrays on FPGAs</strong></td>
</tr>
<tr>
<td>Karel Heyse, Tom Davidson, Elias Vansteenkiste, Karel Bruneel, Dirk Stroobandt</td>
</tr>
<tr>
<td><strong>An Efficient FPGA Overlay for Portable Custom Instruction Set Extensions</strong></td>
</tr>
<tr>
<td>Dirk Koch, Christian Beckhoff, Guy G.F. Lemieux</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Session M3C: Networking Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Session Chair: Teresa Riesgo (Universidade Politécnica de Madrid, Spain)</td>
</tr>
<tr>
<td><strong>A Packet Classifier Using LUT Cascades Based on EVMDDs(k)</strong></td>
</tr>
<tr>
<td>Hiroki Nakahara, Tsutomu Sasao, Munehiro Matsuura</td>
</tr>
<tr>
<td><strong>Memory Efficient IP Lookup in 100 Gbps Networks</strong></td>
</tr>
<tr>
<td>Jiří Matoušek, Martin Skačan, Jan Kořenek</td>
</tr>
<tr>
<td><strong>A Flexible Hash Table Design for 10GBPs Key-Value Stores in FPGAs</strong></td>
</tr>
<tr>
<td>Zsolt István, Gustavo Alonso, Michaela Blott, Kees Vissers</td>
</tr>
</tbody>
</table>
Session T1A: Run-Time Reconfiguration
Session Chair: João Canas Ferreira (FEUP, Universidade do Porto, Portugal)

Weighted Partitioning of Sequential Processing Chains for Dynamically Reconfigurable FPGAs
Michael Feilen, Andreas Iliopoulos, Michael Vonbun, Walter Stechele

Optimizing Under Abstraction: Using Prefetching to Improve FPGA Performance
Hsin-Jung Yang, Kermin Fleming, Michael Adler, Joel Emer

Run-Time Optimization of a Dynamically Reconfigurable Embedded System Through Performance Prediction
Giovanni Mariani, Vlad-Mihai Sima, Gianluca Palermo, Vittorio Zaccaria, Giacomo Marchiori, Cristina Silvano, Koen Bertels

Session T1B: Security Applications
Session Chair: Guy Gogniat (University Bretagne-Sud, France)

A Secure Coprocessor for Database Applications
Arvind Arasu, Ken Eguro, Raghav Kaushik, Donald Kossmann, Ravi Ramamurthy, Ramaratnam Venkatesan

Fast, FPGA-Based Rainbow Table Creation for Attacking Encrypted Mobile Communications
Panos Papantonakis, Charalampos Manifavas, Dionisios Pnevmatikatos, Ioannis Papaefstathiou

FPGA Based ReKeying for Cryptographic Key Management in Storage Area Network
Yi Wang, Yajun Ha

Session T1C: Biosensing and Imaging Applications
Session Chair: Peter Athanas (Virginia Polytechnic Institute, USA)

An FPGA Design for High Speed Feature Extraction from a Compressed Measurement Stream
Dustin Richmond, Ryan Kastner, Ali Irturk, John McGarry

FPGA Implementation of Hierarchical Enumerative Coding for Locally Stationary Image Source
Yuhui Bai, Syed Zahid Ahmed, Bertrand Granado

Scalable and High Throughput Biosensing Platform
José Leitão, José Germano, Nuno Roma, Ricardo Chaves, Pedro Tomás

Session T2A: Floating-Point Arithmetic
Session Chair: Dirk Stroobandt (University of Ghent, Belgium)

Efficient Floating-Point Polynomial Evaluation on FPGAs
Martin Langhammer, Bogdan Pasca

Iterative Floating Point Computation Using FPGA DSP Blocks
Fredrik Brosser, Hui Yan Cheah, Suhail Fahmy

Session T2B: Fault-Tolerance and Scrubbing
Session Chair: Minoru Watanabe (Shizuoka University, Japan)

Radiation Mitigation Efficiency of Scrubbing on the FPGA Based CBM-ToF Read-Out Controller
Sebastian Manz, Jano Gebelein, Andrei Oancea, Heiko Engel, Udo Kebschull

Accelerated FPGA Repair through Shifted Scrubbing
Gabriel Nazar, Leonardo P. Santos, Luigi Carro
<table>
<thead>
<tr>
<th>Session T2C: Pattern Matching Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Session Chair: Viktor Prasanna (University Southern California, USA)</td>
</tr>
<tr>
<td><strong>Hardware-Accelerated Regular Expression Matching for High-Throughput Text Analytics</strong></td>
</tr>
<tr>
<td>Kubilay Atasu, Raphael Polig, Christoph Hagleitner, Frederick. R. Reiss</td>
</tr>
<tr>
<td><strong>Token-Based Dictionary Pattern Matching for Text Analytics</strong></td>
</tr>
<tr>
<td>Raphael Polig, Kubilay Atasu, Christoph Hagleitner</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Session W1A: Soft Processor Systems and Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Session Chair: Markus Weinhardt (Osnabrück Hochschule, Germany)</td>
</tr>
<tr>
<td><strong>Low-Cost, High-Performance Branch Predictors for Soft Processors</strong></td>
</tr>
<tr>
<td>Di Wu, Kaveh Aasaraai, Andreas Moshovos</td>
</tr>
<tr>
<td><strong>TputCache: High-Frequency, Multi-Way Cache for High-Throughput FPGA Applications</strong></td>
</tr>
<tr>
<td>Aaron Severance, Guy Lemieux</td>
</tr>
<tr>
<td><strong>Managing the FPGA Memory Wall: Custom Computing or Vector Processing?</strong></td>
</tr>
<tr>
<td>Matthew Naylor, Paul J. Fox, A. Theodore Markettos, Simon W. Moore</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Session W1B: High-Level Synthesis and CAD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Session Chair: David Andrews (University of Arkansas, USA)</td>
</tr>
<tr>
<td><strong>Rapid FPGA Design Prototyping Through Preservation of System Logic: A Case Study</strong></td>
</tr>
<tr>
<td>Travis Haroldsen, Brent Nelson, Brad White</td>
</tr>
<tr>
<td><strong>Dynamic Branch Prediction for High-Level Synthesis</strong></td>
</tr>
<tr>
<td>Vianney Lapotre, Philippe Coussy, Cyrille Chavet, Hugo Wouafo, Robin Danilo</td>
</tr>
<tr>
<td><strong>High-Level Synthesis with Behavioral Level Multi-Cycle Path Analysis</strong></td>
</tr>
<tr>
<td>Hongbin Zheng, Swathi Gurumani, Liwei Yang, Deming Chen, Kyle Rupnow</td>
</tr>
<tr>
<td><strong>Simulation-Based HW/SW Co-Debugging for Field-Programmable Systems-On-Chip</strong></td>
</tr>
<tr>
<td>Ruediger Willenberg, Paul Chow</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Session W1C: Arithmetic and Computation Cores</th>
</tr>
</thead>
<tbody>
<tr>
<td>Session Chair: Tim Todman (Imperial College London, UK)</td>
</tr>
<tr>
<td><strong>Multiple Constant Multiplication with Ternary Adders</strong></td>
</tr>
<tr>
<td>Martin Kumm, Martin Hardieck, Jens Willkomm, Peter Zipf, Uwe Meyer-Baese</td>
</tr>
<tr>
<td><strong>Arithmetic Core Generation Using Bit Heaps</strong></td>
</tr>
<tr>
<td>Nicolas Brunie, Florent de Dinechin, Kinga Illyes, Matei Istoan, Bogdan Popa</td>
</tr>
<tr>
<td><strong>Energy Efficient Parameterized FFT Architecture</strong></td>
</tr>
<tr>
<td>Ren Chen, Hoang Le, Viktor K. Prasanna</td>
</tr>
<tr>
<td><strong>Area/Performance Evaluation of Digit-Digit GF(2^k) Multipliers on FPGAs</strong></td>
</tr>
<tr>
<td>Miguel Morales-Sandoval, Arturo Díaz-Pérez</td>
</tr>
</tbody>
</table>
Short Papers (Poster Session #2)
Session Chair: Eduardo Marques (ICMC, Universidade de São Paulo, Brazil)

A Directional Coarse-Grained Power Gated FPGA Switch Box and Power Gating Aware Routing Algorithm
Chin Hau Hoo, Yajun Ha and Akash Kumar

Dependable Dynamic Partial Reconfiguration with Minimal Area & Time Overheads on Xilinx FPGAs
Stefano Di Carlo, Giulio Gambardella, Marco Indaco, Paolo Prinetto, Daniele Rolfo and Pascal Trotta

Bambu: A Modular Framework for the High Level Synthesis of Memory-Intensive Applications
Christian Pilato and Fabrizio Ferrandi

A Scalable Design Approach for Stencil Computation on Reconfigurable Clusters
Xinyu Niu, Jose G. F. Coutinho and Wayne Luk

Comparing and Combining GPU and FPGA Accelerators in an Image Processing Context
Bruno da Silva, An Braeken, Erik H. D’Hollander, Abdellah Touhafi, Jan G. Cornelis and Jan Lemeire

TILT: A Multithreaded VLIW Soft Processor Family
Kalin Ovtcharov, Ilian Tili and J. Gregory Steffan

FPGA Based Hardware-Software Co-Designed Dynamic Binary Translation System
Yuan Yao, Zhongyong Lu, Qingsong Shi and Wenzhi Chen

FPGA IP Protection by Binding Finite State Machine to Physical Unclonable Function
Jiliang Zhang, Yaping Lin, Yongqiang Lyu, Gang Qu, Ray C.C. Cheung, Wenjie Che, Qiang Zhou and Jinian Bian

A Hardware Security Scheme for RRAM-based FPGA
Yi-Chung Chen, Wei Zhang and Hai Li

Accurate and Flexible Flow-Based Monitoring for High-Speed Networks
Marco Forconesi, Gustavo Sutter, Sergio Lopez-Buedo and Javier Aracil

A High-Performance IPV6 Lookup Engine on FPGA
Thilan Ganegedara and Viktor Prasanna

High Performance Architecture for Object Detection in Streamed Videos
Pavel Zemcik, Roman Juranek, Petr Musil, Martin Musil and Michal Hradis

FPGA-Accelerated Sliding Window Classifier with Structured Features
Ondrej Sychrovsky, Martin Matousek and Radim Sara

Performance Evaluation of Sparse Matrix-Matrix Multiplication
Shweta Jain-Mendon and Ron Sass

Aging-Based Leakage Energy Reduction in FPGAs
Sheng Wei, Jason Zheng and Miodrag Potkonjak
**Short Papers (Poster Session #3)**

Session Chair: João Bispo (FEUP, Universidade do Porto, Portugal)

**A Novel Net-Partition-Based Multithread FPGA Routing Method**  
Chun Zhu, Jian Wang and Jinmei Lai  

**A Platform-Independent Runtime Methodology for Mapping Multiple Applications onto FPGAs Through Resource Virtualization**  
Harry Sidiropoulos, Peter Figuli, Kostas Siozios, Dimitrios Soudris and Jürgen Becker  

**Timing-Constrained Minimum Area/Power FPGA Memory Mapping**  
Fangqing Du, Colin Yu Lin, Xiuhai Cui, Feng Liu, Fei Liu and Haigang Yang  

**Shadow And-Inverter Cones**  
Hadi Parandeh-Afshar, Grace Zgheib, David Novo, Madhura Purnaprajna and Paolo Ienne  

**Analyzing the Thermal Hotspots in FPGA-Based Embedded Systems**  
Hussam Amrouch, Thomas Ebi, Josef Schneider, Sridevan Parameswaran and Jörg Henkel  

**Energy Efficient Architecture for Matrix Multiplication on FPGAs**  
Kiran Matam, Hoang Le and Viktor Prasanna  

**An Asynchronous Bus Bridge for Partitioned Multi-SoC Architectures on FPGAs**  
Daniel Kliem and Sven-Ole Voigt  

**An Open-Source Multi-FPGA Modular System for Fair Benchmarking of True Random Number Generators**  
Viktor Fischer, Patrick Haddad and Florent Bernard  

**Towards Bounded Error Recovery Time in FPGA-based TMR Circuits using Dynamic Partial Reconfiguration**  
Ediz Cetin, Oliver Diessel, Lingkan Gong and Victor Lai  

**Compact Implementation of CCM and GCM modes of AES using DSP blocks**  
Antonio de la Piedra, Abdellah Touhafi and An Braeken  

**Design of a Multi GBPS Single Carrier Digital Baseband for 60GHz Applications and its FPGA Implementation**  
Surendra Guntur, Feike Jansen, Jan Hoogerbrugge, Lotfi Abkari and Eric Vos  

**A Single-Precision Compressive Sensing Signal Reconstruction Engine on FPGAs**  
Fengbo Ren, Richard Dorrance, Wenyao Xu and Dejan Marković  

**A Study of a Three-Dimensional Multiphase-Flow Simulator**  
Kenta Fujinami, Yoshiki Yamaguchi, Akira Sugiuira and Yuetsu Kodama  

**Weasel: A Platform-Independent Streaming-optimized SATA Controller**  
Patrick Lehmann, Thomas Frank, Oliver Knodel, Steffen Köhler, Thomas B. Preußner and Rainer G. Spallek
Short Papers (Poster Session #4)

Session Chair: Nuno Roma (Instituto Superior Técnico /INESC-ID, Portugal)

A Variation-Adaptive Retiming Method Exploiting Reconfigurability
Zhenyu Guan, Justin S. J. Wong, Sumanta Chaudhuri, George Constantinides and Peter Y. K. Cheung

An Event-Based Middleware for the Remote Management of Runtime Hardware Reconfiguration
François Philipp and Manfred Glesner

Timing Driven RTL-to-RTL Partitioner for Multi-FPGA Systems
Tobias Strauch

Shared Memory Heterogeneous Computation on PCIe-supported Platforms
Sambit Shukla, Yang Yang, Laxmi Bhuyan and Philip Brisk

A Resource-Efficient Probabilistic Fault Simulator
David May and Walter Stechele

Generation of Multi-Core Systems from Multithreaded Software
Alexander Wold, Jim Tørresen and Andreas Agne

Design Space Explorations of Hybrid-Partitioned TCAM (HP-TCAM)
Zahid Ullah, Manish Kumar Jaiswal and Ray C.C. Cheung

On Measurement of Parameters of Programmable Microelectronic Nanostructures Under Accelerating Extreme Conditions
Petr Pfeifer and Zdenek Pliva

Hardware-efficient Implementation of a Femtocell/Macrocell Interference-Mitigation Technique for High-performance LTE-Based Systems
Oriol Font-Bach, Nikolaos Bartzoudis, Miquel Payaró and Antonio Pascual-Iserte

A CMOS FIELD Programmable Analog Array for Intelligent Sensory Application
Cheng Xiaoyan, Yin Tao, Wu Qisong and Yang Haigang

A Low-Complexity Implementation of QC-LDPC Encoder in Reconfigurable Logic
Georgios Tzinpragos, Christoforos Kachris, Dimitrios Sourdris and Ioannis Tomkos

Fast Dynamically Updatable Packet Classifier on FPGA
Yun Qu and Viktor Prasanna

A Digital Architecture for Real-time Nonuniformity Correction of Infrared Focal-Plane Arrays
Rodolfo Redlich and Miguel Figueroa

Binarization Based Implementation for Real-time Human Detection
Shuai Xie, Yibin Li, Zhiping Jia and Lei Ju

Magnitude Modulation on Reconfigurable Computing Devices
Marco Gomes, Vitor Silva and Ricardo Ferrão
Short Papers (Poster Session #5)

Session Chair: Ricardo Chaves (Instituto Superior Técnico /INESC-ID, Portugal)

Yet Another Many-Objective Clustering (YAMO-PACK) for FPGA CAD
Meng Yang, Jinmei Lai and Jiarong Tong

An Automatic FPGA Design and Implementation Framework
Qian Zhao, Motoki Amagasaki, Masahiro Iida, Morihiro Kuga and Toshinori Sueyoshi

A Hardware Complete Detection Mechanism for an Energy Efficient Reconfigurable Accelerator CMA
Akihito Tsusaka, Mai Izawa, Roe Uno, Nobuyuki Ozaki and Hideharu Amano

Towards a Many-Core Architecture for HPC
Janet Wyngaard, John Collins, Brian Farrimond and Michael Inggs

Aging Monitoring with Local Sensors in FPGA-Based Designs
Carlos Leong, Jorge Semião, Isabel Teixeira, Marcelino Santos, M. Valdés, Judit Freijedo, J. Rodriguez, F. Vargas, João Teixeira

Runtime Assertions and Exceptions for Streaming Systems
Tim Todman and Wayne Luk

SMI: Slack Measurement Insertion for Online Timing Monitoring in FPGAs
Joshua M. Levine, Edward Stott, George A. Constantinides and Peter Y.K. Cheung

Pedro Vieira dos Santos, José Carlos Alves and João Canas Ferreira

SDR Control Interface: An FPGA Based Infrastructure for Control of VPX Software Defined Radio Systems
Stefanie Castillo, Armando Astarloa, Jesus Lazaro, Sergio Salas and Isaac Ballesteros

Design and FPGA Implementation of a 100 Gbit/s Optical Transport Network Processor
Rodrigo Bernardo, Arley Henrique Salvador, Eduardo Mobilon, Luis Renato Monte, Stephane Boisclair, Avrum Warshawsky

A High Performance Deblocking Filter Hardware for High Efficiency Video Coding
Erdem Ozcan, Yusuf Adibelli and Ilker Hamzaoglu

Image Recognition Operation on a Dynamically Reconfigurable Vision Architecture
Yuki Kamikubo, Minoru Watanabe and Shoji Kawahito

Analysis of Matrix Multiplication on High Density Virtex-7 FPGA
Wilson Maltez, Ana Rita Silva, Horácio Neto and Mário Véstias

FPGA Implementation and DPA Resistance Analysis of a Lightweight HMAC Construction Based on Photon Hash Family
Susana Eiroa and Iluminada Baturone

FEMIP: A High Performance FPGA-Based Features Extractor & Matcher for Space Applications
Stefano Di Carlo, Giulio Gambardella, Piergiorgio Lanza, Paolo Prinetto, Daniele Rolfo and Pascal Trotta
Short Papers (PhD Forum, Poster Session)

Session Chair: Stephan Wong (TU Delft, The Netherlands)

**Design Space Exploration based on MultiObjective Genetic Algorithms and Clustering-based High-Level Estimation**  
Luiz Martins and Eduardo Marques

**A Dataflow-Inspired CGRA for Streaming Applications**  
Anja Niedermeier, Jan Kuper and Gerard J.M. Smit

**FPGA Based Control for Real Time Systems**  
Shane Fleming and David Thomas

**Pipelining Computing Stages in Configurable Multicore Architectures**  
Ali Azarian

**Integration of a Multi-FPGA System in a Common Cluster Environment**  
Oliver Knodel and Rainer Spallek

**A Space/Time Tradeoff Methodology Using Higher-Order Functions**  
Rinse Wester and Jan Kuper

**Degradation in FPGAs: Monitoring, Modeling and Mitigation**  
Abdulazim Amouri and Mehdi Tahoori

**Identifying Sequences of Optimizations for HW/SW Compilation**  
Ricardo Nobre

**A Reconfigurable Computing Architecture Using Magnetic Tunneling Junction Memories**  
Victor Silva, Jorge Fernandes, Mário Véstias and Horácio Neto

**Distributed Embedded Systems Design Using Petri Nets**  
Filipe Moutinho and Luis Gomes
Short Papers (Demo Presentations)

Chair: José G. F. Coutinho (Imperial College London, UK)

**Hybrid FPGA-Accelerated SQL Query Processing**
Louis Woods, Zsolt István and Gustavo Alonso

**Rapid Modular Assembly of Xilinx FPGA Designs**
Andrew Love and Peter Athanas

**Remote FPGA Design Through eDiViDe - European Digital Virtual Design Lab**
Jochen Vandorpe, Jo Vliegen, Ruben Smeets, Nele Mentens, Milos Drutarovsky, Michal Varchola, Kerstin Lemke-Rust, Peter Samarin, Paul Plöger, Dirk Koch, Yngve Hafting and Jim Tørresen

**High Performance FPGA Object Detector**
Pavel Zemčík, Roman Juránek, Petr Musil, Martin Musil and Michal Hradiš

**MAMPSx: A Demonstration of Rapid, Predictable HMPSoC Synthesis**
Shakith Fernando, Mark Wijtvliet, Firew Siyoum, Yifan He, Sander Stuijk, Akash Kumar and Henk Corporaal

**NetThreads-10G: Software Packet Processing on NetFPGA-10G in a Virtualized Networking Environment**
Stuart Byma, J. Gregory Steffan and Paul Chow

**Parallel and Scalable Custom Computing for Real-Time Fluid Simulation on a Cluster Node with Four Tightly-Coupled FPGAs**
Kentaro Sano, Ryo Ito, Hayato Suzuki and Yoshiaki Kono

**From Quartus to VPR: Converting HDL to BLIF with the Titan Flow**
Kevin E. Murray, Scott Whitty, Suya Liu and Vaughn Betz

**The HercuLeS High-Level Synthesis Environment**
Nikolaos Kavvadias and Kostas Masselos

**Demonstration of a Heterogeneous Multi-Core Processor with 3-D Inductive Coupling Links**
Yusuke Koizumi, Noriyuki Miura, Yasuhiro Take, Hiroki Matsutani, Tadahiro Kuroda, Hideharu Amano, Ryuichi Sakamoto, Mitaro Namiki, Kimiyoshi Usami, Masaaki Kondo and Hiroshi Nakamura

**A Spiking Neural Network on a Portable FPGA Tablet**
Matthew Naylor, Paul J Fox, A Theodore Markettos and Simon W Moore

**A 64-bit MIPS Processor Running FreeBSD on a Portable FPGA Tablet**
Jonathan Woodruff, A. Theodore Markettos and Simon W Moore

**A Self-Adaptive Image Processing Application Based on Evolvable and Scalable Hardware**
Ángel Gallego, Javier Mora, Andrés Otero, Blanca López, Eduardo de la Torre and Teresa Riesgo

**SimXMD: Simulation-Based HW/SW Co-Debugging**
Ruediger Willenberg and Paul Chow

Luis Gomes, Filipe Moutinho, and Fernando Pereira

**Building Partial Systems with GOAHEAD**
Christian Beckhoff, Alexander Wold, Anders Fritzell, Dirk Koch and Jim Tørresen