2013 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S 2013)

(Formerly known as SOI Conference)

Monterey, California, USA
7-10 October 2013
# General Chair’s Welcome Message

<table>
<thead>
<tr>
<th>Committee List</th>
<th>Introduction and History</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technical Sessions:</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Session 1:</strong> Plenary Session</td>
<td><strong>Session 6b:</strong> Sub Vt - Digital 3</td>
</tr>
<tr>
<td><strong>Session 2a:</strong> SOI FinFET</td>
<td><strong>Session 7:</strong> Joint Poster Session</td>
</tr>
<tr>
<td><strong>Session 2b:</strong> Sub Vt - Analog &amp; RF</td>
<td><strong>Session 8a:</strong> SOI Memory</td>
</tr>
<tr>
<td><strong>Session 3a:</strong> SOI Substrates</td>
<td><strong>Session 8b:</strong> Sub Vt - Microcontrollers and Memory</td>
</tr>
<tr>
<td><strong>Session 3b:</strong> Sub Vt - Digital 1</td>
<td><strong>Session 9a:</strong> Novel SOI Devices</td>
</tr>
<tr>
<td><strong>Session 4:</strong> Special Invited Hot Topics RF Session</td>
<td><strong>Session 9b:</strong> Sub-Vt Devices</td>
</tr>
<tr>
<td><strong>Session 5a:</strong> SOI Circuit Design</td>
<td><strong>Session 10:</strong> Hot Topics: 3DI</td>
</tr>
<tr>
<td><strong>Session 5b:</strong> Sub Vt - Digital 2</td>
<td><strong>Session 11:</strong> Late News</td>
</tr>
<tr>
<td><strong>Session 6a:</strong> FDSOI</td>
<td><strong>Author Index</strong></td>
</tr>
</tbody>
</table>

Sponsored by the IEEE Electron Devices Society
List of Presentations

SESSION 1  PLENARY SESSION  SESSION CHAIRS
Bruce Doris, IBM
Steven Vitale, MIT Lincoln Labs
Subramanian Iyer, IBM

1.1 Fully-Depleted-Silicon-On-Insulator From R&D Concept to Industrial Reality
L. Le Pailleur; ST Microelectronics (invited talk)

1.2 The Past and Future of Low Power CMOS Design
B. Brodersen¹, A. Chandrakasan²; ¹University of California at Berkeley, ²Massachusetts Institute of Technology (invited talk)

1.3 Practical Process Flows for Monolithic 3D
Z. Or-Bach; Monolith IC3D, San Jose, USA (invited talk)

SESSION 2a  SOI FinFET  SESSION CHAIRS
Bich-Yen Nguyen, Soitec
Changhwan Shin, University of Seoul

2a.1 FinFETs for the Future
A. Bryant, E. Nowak, T. Hook; IBM, Albany, USA (invited talk)

2a.2 Fin Width Scaling for Improved Short Channel Control and Performance in Aggressively Scaled Channel Length SOI FinFETs
A. Paul¹, C.-C. Yeh, T. Standaert, J.B. Johnson², A. Bryant, N. Tripathi¹, G. Tsutsui, T. Yamashita, V. S. Basker, J. Faltermeier, J. Cho¹, H. Bu and M. Khare; ¹GLOBALFOUNDRIES, Inc. Albany, USA, ²IBM Research, Albany, USA

2a.3 Influence of Substrate Rotation on the Low Frequency Noise of Strained Triple-Gate MuGFETs
M.A.S. de Souza¹, R.T. Doria², E. Simoen³, J.A. Martino¹, C. Ca ley², and M.A. Pavanello²,³; ¹LSI/PSI/USP, University of São Paulo, São Paulo, Brazil, ²Electrical Engineering Department, Centro Universitário da FEI, São Bernardo do Campo, Brazil, ³imec, Leuven, Belgium, ⁴E.E. Department, KU Leuven, Leuven, Belgium

2a.4 Comparative Simulation of TriGate and FinFET on SOI: Evaluating a Multiple Threshold Voltage Strategy on Triple Gate Devices
R. Coquand¹,²,³, M.-A. Jaud², O. Rozeau², A. Idrissi-El Oudrihi², S. Martinie², F. Trizo n², N. Pons², S. Barraud², S. Monfray¹, F. Boeuf¹, G. Ghibaudo², O. Faynot²; ¹STMicroelectronics Crolles, France, ²CEA-LETI, MINATEC Campus, Grenoble, France, ³IMEP-LAHC, Grenoble France
2b.1 **Enabling Sub-nW RF Circuits through Subthreshold Leakage Management**  
P.P. Mercier¹, S. Bandropadhyay², A. P. Chandrakasan³; ¹University of California San Diego, La Jolla, USA, ²Texas Instruments, Dallas, USA, ³Massachusetts Institute of Technology, Cambridge, USA (invited paper)

2b.2 **280mV Sense Amplifier Designed in 28nm UTBB FD-SOI Technology Using Back-Biasing Control**  
A. Feki¹, D. Turgis¹, J.C. Lafont¹, B. Allard²; ¹STMicroelectronics Crolles France, ²University of Lyon, INSA-Lyon, Villeurbanne, France

2b.3 **Low Power False Positive Tolerant Event Detector for Seismic Sensors**  
U. Antao¹, A. Dibazar¹, J. Choma¹, T. Berger²; ¹Ming Hsieh Department of Electrical Engineering, University of Southern California, Los Angeles, USA, ²Department of Biomedical Engineering, University of Southern California, Los Angeles, USA

2b.4 **Enabling Energy Efficient Protocol Processing for Passive RFID Sensors Using Sub/Near-Threshold Circuit**  
R. Liao¹, R. Ahmed¹, C.G. Hutchens¹ and R.L. Rennaker II²; ¹Oklahoma State University, Stillwater, USA; ²University of Texas, Dallas, Dallas, USA

---

3a.1 **Substrate Solutions to Address the Smart Handheld Low Power Demands**  
C. Mazure; Soitec, Bernin, France (invited talk)

3a.2 **Opportunities in 3D Substrate Bonding**  
T. Matthias, T. Uhrmann, V. Dragoi and P. Lidner; EV Group (invited talk)

3a.3 **Direct Point-Contact Characterization of Bias Instability on Bare SOI Wafers**  
C. Marquez¹, N. Rodriguez¹, C. Fernandez¹, A. Ohata², F. Gamiz¹, F. Allibert¹, S. Cristoloveanu²; ¹Nanoelectronics Research Group, Universidad de Granada, Granada, Spain, ²IMEP-LAHC, MINATEC, Grenoble, France, ³Soitec, Crolles, France

3a.4 **Radiation Effects in Advanced SOI Devices: New Insights into Total Ionizing Dose and Single-Event Effects**  
M. Gaillardin¹, M. Raine¹, P. Paillet¹, M. Martinez¹, C. Marcandella¹, S. Girard², O. Duhamel¹, N. Richard¹, F. Andreiu³, S. Barraud³, O. Faynot¹; ¹CEA DAM DIF, Arpajon, France, ²Université Jean Monnet Saint-Etienne, France, ³CEA-LET Minatec, Grenoble, France (invited talk)
### SESSION 3b  Sub Vt - Digital I  SESSION CHAIR  John Ahlbin, ISI

<table>
<thead>
<tr>
<th>Session</th>
<th>Title</th>
<th>Authors</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>3b.1</td>
<td>Energy Efficient 0.5V Logic, RF and Power Management Circuits</td>
<td>M. Takamiya; <em>University of Tokyo, Tokyo, Japan</em> (invited talk)</td>
<td></td>
</tr>
<tr>
<td>3b.2</td>
<td>Hold Time Closure for Subthreshold Circuits Using a Two-Phase, Latch Based Timing Method</td>
<td>Y. Zhang and B.H. Calhoun; <em>University of Virginia, USA</em></td>
<td></td>
</tr>
<tr>
<td>3b.3</td>
<td>Ultra Low Power 2-tier 3D Stacked Sub-threshold H.264 Intra Frame Encoder</td>
<td>S.K. Samal¹, K. Kim², Y. Kim², T. Kim², H.-J. Lee², T. Kim² and S.K. Lim¹; ¹School of ECE, Georgia Institute of Technology, Atlanta, USA, ²School of ECE Seoul National University, Seoul, Korea,</td>
<td></td>
</tr>
</tbody>
</table>

### SESSION 4  Special Invited Hot Topics RF Session  SESSION CHAIR  Carlos Mazure, Soitec

<table>
<thead>
<tr>
<th>Session</th>
<th>Title</th>
<th>Authors</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1</td>
<td>Is High Resistivity SOI Wafer the Substrate Solution for RF System-on-Chip?</td>
<td>J. P. Raskin; <em>Université catholiques de Louvain, Louvain-la-Neuve, Belgium</em> (invited talk)</td>
<td></td>
</tr>
<tr>
<td>4.2</td>
<td>Envelope Tracking Power Amplifier Optimization for Mobile Applications</td>
<td>J. P. Young, D. Ripley and P. Lehtola; <em>Skyworks Solution Inc. Cedar Rapids, USA</em> (invited talk)</td>
<td></td>
</tr>
<tr>
<td>4.3</td>
<td>Foundry SOI Technology for Wireless Front-End-Modules</td>
<td>P. Hurwitz, S. Chaudry, V. Blaschke and M. Racanelli; <em>TowerJazz, Newport Beach, USA</em> (invited talk)</td>
<td></td>
</tr>
<tr>
<td>4.4</td>
<td>MEMS Solutions in RF Applications</td>
<td>V. Joshi, R. Parkhurst, L. Morrell and P. Tornatta; <em>Cavendish Kinetics, San Jose, USA</em> (invited talk)</td>
<td></td>
</tr>
<tr>
<td>4.5</td>
<td>The State-of-the-Art of RF Front-End Integration in SOI CMOS</td>
<td>D. Kelly, D. Nobbe, C. Olson; <em>Peregrine</em> (invited talk)</td>
<td></td>
</tr>
</tbody>
</table>

### SESSION 5a  SOI Circuit Design  SESSION CHAIRS  Keiji Ikeda, AIST  Toshiro Hiramoto, University of Tokyo

<table>
<thead>
<tr>
<th>Session</th>
<th>Title</th>
<th>Authors</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>5a.1</td>
<td>Simulation of Statistical Variability in Nanometer Scale CMOS Devices</td>
<td>A. Asenov; <em>Gold Standard Simulations Ltd. and the University of Glasgow, Glasgow, U.K.</em> (invited talk)</td>
<td></td>
</tr>
<tr>
<td>5a.2</td>
<td>A Trench Isolated Thick SOI Process as Platform for Various Electrical and Optical Integrated Devices</td>
<td>R. Lerner, D. Gaebler, K. Schottmann and S. Hering; <em>X-FAB Semiconductor Foundries AG, Erfurt, Germany</em></td>
<td></td>
</tr>
</tbody>
</table>
5a.3  Evaluation of Transient Voltage Collapse Write-Assist for GeOI and SOI FinFET SRAM Cells  48
V.P.-H. Hu, M.-L. Fan, P. Su and C.-T. Chuang; Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Taiwan

5a.4  Robust Clock Tree Using Single-Well Cells for Multi-VT 28nm UTBB FD-SOI Digital Circuits  50
B. Giraud1, J.P. Noel2, F. Abouzeid2, S. Clerc2 and Y. Thonnart1; 1CEA-LETI, MINATEC, Grenoble, France, 2STMicroelectronics, Crolles, France

5a.5  The First SOTB Implementation of Flex Power FPGA  52
H. Koike1, C. Ma1,2, M. Hioki1, Y. Ogasahara1, T. Kawanami1, T. Tsutsumi2, T. Nakagawa1 and T. Sekigawa1; 1National Institute of AIST, 2Meiji University, Japan

5a.6  DTMOS Power Switch in 28 nm UTBB FD-SOI Technology  54
J. Le Coz1, B. Pelloux-Prayer1, B. Giraud2, F. Giner1, P. Flatresse1; 1STMicroelectronics, Crolles, France 2CEA-LETI, Minatec Campus, Grenoble, France

SESSION 5b  Sub Vt - Digital 2  SESSION CHAIR
Yang Du, Qualcomm

5b.1  Moving Subthreshold from the Lab to Production: Past and Future Challenges  N/A
S. Hanson; Ambiq Micro (invited talk)

5b.2  High Temperature and Radiation Hard CMOS SOI Sub-threshold Voltage Reference  56
E. Boufouss, P. Gérard, P. Simon, L.A. Francis and D. Flandre; MICTEAM Institute, Université catholique de Louvain, Louvain-la-Neuve, Belgium

5b.3  Dual-Threshold Design of Sub-threshold Circuits  58
J. Yao, V. D. Agrawal; Department of ECE, Auburn University, Auburn, USA

5b.4  Performance Characteristics of 14nm Near Threshold MCML Circuits  60
A. Shapiro and E.G. Friedman; Department of Electrical Engineering, University of Rochester, Rochester, USA

5b.5  Asynchronous-logic: Low-Power/Ultra Low-Power Design, and High Variation-space Wide Operation-space Applications  N/A
J. Chang1, T. Lin2, K.-S. Chong2; 1Nanyang Technological University, Singapore, 2Temasek Labs, Nanyang Technological University, Singapore (invited talk)
6a.1 UTBB FDSOI Scaling Enablers for the 10nm Node  62

6a.2 Matching Behavior of Analog FDSOI n-MOS-Transistors Under Large Backgate Voltage Swing Operating Conditions  64
R. Thewes1,2, G. Enders1, F. Hofmann1, W. Hoenle1, J. Vollrath1,3, R. Ferrant4, P. Flattesse2, B. Pelloux-Prayer1, F. Allain6, G. Reimbold6 and C. Mazure7; 1Memory Consultant, Munich, Germany, 2TU Berlin, Berlin, Germany, 3UAS Kempten, Kempten, Germany, 4formerly Soitec, Bernin, France 5STMicroelectronics, Grenoble, France, 6CEA-LETI, Grenoble, France 7Soitec, Bernin, France

6a.3 Performance Analysis of Multi-VT Design Solutions in 28nm UTBB FDSOI Technology  66
B. Pelloux-Prayer1, M. Blagojevic1, S. Haendler1, A. Valentain2, A. Amara1 and P. Flattesse1; 1ST Microelectronics, Crolles, France, 2CEA-LETI, MINATEC Campus, Grenoble, France, 3ISEP, Paris, France

6a.4 Self-Aligned Contacts for 10nm FDSOI Node: From Device to Circuit Evaluation  68
H. Niebojewski1, C. Le Royer2, Y. Morand1, O. Rozeau2, M.-A. Jaud2, S. Barnola2, C. Arvet1, J. Pradelles2, J. Bustos1, J.M. Pedini1, E. Dubois3 and O. Faynot4; 1STMicroelectronics, Crolles, France, 2CEA-LETI, MINATEC Campus, Grenoble, France

6a.5 Possibility of SOI Based Super Steep Subthreshold Slope MOSFET for Ultra Low Voltage Application  70
T. Moria and J. Ida; Department of Electrical and Electronic Engineering, Kanazawa Institute of Technology, Nonoichi Ishikawa, Japan

6a.6 Evidence of Mobility Enhancement Due to Back Biasing in UTBOX FDSOI High-k Metal Gate Technology  72
I. Ben Akkez1,2,3, C. Fenouillet-Beranger3,1, A. Cros3, F. Balestra2, G. Ghibaudo2; 1STMicroelectronics, Crolles, France, 2IMEP-LAHC, MINATEC Campus, Grenoble, France, 3CEA-LETI, MINATEC Campus, Grenoble, France

6b.1 Parallelism and Pipelining in Ultra-Low Voltage Digital Circuits  74
M. Seok, Z. Cao; Department of Electrical Engineering, Columbia University, New York, USA (invited talk)

6b.2 Scaling Perspectives of ULV Microcontroller Cores to 28nm UTBB FDSOI CMOS  76
G. de Street and D. Bol; ICTEAM Institute, Université catholique de Louvain, Louvain-la-Neuve, Belgium
6b.3 Delay Insensitive Logic with Increased Fault Tolerance and Optimized for Subthreshold Operation  78
I. Santos and E. MacDonald; The University of Texas at El Paso, El Paso, USA

6b.4 Design of a Robust and Ultra-Low-Voltage Pulse-Triggered Flip-Flop in 28nm UTBB-FDSOI Technology  80
S. Bernard1, A. Valentian1, M. Belleville1, D. Bo1, J.-D. Legat2; 1CEA-LETI, MINATEC, Grenoble, France, 2ICTEAM Université catholique de Louvain, Louvain-la-Neuve, Belgium

6b.5 Adaptive and Resilient Circuits for Improving Energy Efficiency in Wide Dynamic Range Digital Systems  N/A
A. Raychowdhury; Georgia Tech (invited talk)

SESSION 7 Joint Poster Session
SESSION CHAIR
Michel Haond, STMicroelectronics

7.1 A Sub-Threshold Halo Implanted MOS Implementation of Izhikevich Neuron Model  82
O.O. Dutra, G.D. Colleta, L.H.C. Ferreira and T.C. Pimenta; Systems Engineering and Information Technology Institute, Federal University of Itajubá, Brazil

7.2 An Ultra-Low-Power First-Order Asynchronous Sigma-Delta Modulator for Biomedical Applications  84
G. D. Colletta, O.O. Dutra, L.H. Ferreira and T.C. Pimenta; Systems Engineering and Information Technology Institute, Federal University of Itajubá, Brazil

7.3 A Double-Feedback 8T SRAM Bitcell for Low-Voltage Low-Leakage Operation  86
A. Vaknin, O. Yona and A. Teman; VLSI Systems Center, Ben-Gurion University of the Negev, Be’er Sheva, Israel

7.4 A Low Power and Radiation-Tolerant FPGA Implemented in FD SOI Process  88
L. Wu, G. Zhang, Y. Zhao, X. Han, B. Yang, J. Li, J. Wang, J. Gao, K. Zhao, N. Li, F. Yu, Z. Liu; Institute of Microelectronics of Chinese Academy of Sciences

7.5 Demonstration of Gate-All-Around FETs Based on Suspended CVD-Grown Silicon Nanowires  90
J. Y. Oh1, S.-M. Lee3, J.-T. Park1, M. Triplett2,1, D. Yu2 and M. S. Islam1; 1Electrical and Computer Engineering, University of California Davis, Davis, USA, 2Department of Physics, University of California Davis, Davis, USA, 3Electronics Engineering, University of Incheon, Incheon, Republic of Korea

7.6 Experimental Comparative Study Between the Diamond MOSFET and Its Conventional Counterpart in High Temperatures Environment  92
E.H.S. Galembeck1, C. Renaux2, D. Flandre2 and S.P. Gimenez1; 1FEI, São Bernardo do Campo, Brazil, 2 ICTEAM/ELEN, Université catholique de Louvain, Louvain-la-Neuve, Belgium

7.7 Harmonic Distortion Analysis of Short Channel Junctionless Nanowire Transistors Operating as Amplifiers  94
R.T. Doria, R.D. Trevisoli, M. de Souza and M.A. Pavanello; Centro Universitário da FEI, São Bernardo do Campo, Brazil

7.8 The Activation Energy Dependence on the Electric Field in UTBOX SOI FBRAM Devices  96
T. Nicoletti1, S.D. Santos1, K.R.A. Sasaki1, J.A. Martino1, M. Aoulaiche3, E. Simoen5, C. Claeyss2,3, 1LSI/PSI/USP, University of São Paulo, São Paulo, Brazil, 2imec, Leuven, Belgium, 3imec, Leuven, Belgium, 5Department of Electrical Engineering, KU Leuven, Belgium

2013 IEEE S3S Conference | Monterey, CA USA
Germanium on Insulator (GOI) Structure Locally Grown on Silicon Using Hetero Epitaxial Lateral Overgrowth  98
J.H. Nam1, W.S. Jung1, J. Shim2, T. Ito1, Y. Nishi1, J.-H. Park2 and K.C. Saraswat1; 1Department of Electrical Engineering, Stanford University, Stanford, USA, 2Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, Korea

Gate Length Scaling of High-k Vertical MOSFET Toward 20nm CMOS Technology and Beyond  100
T. Sasaki1,2 and T. Endoh1,2; 1Graduate School of Engineering, Tohoku University, Sendai, Japan, 2JST-CREST

Thermal Stability of Ultra-Thin InGaAs-on-Insulator  102
N. Daix, L. Czornomaz, D. Caimi, C. Rossel, M. Sousa and J. Fompeyrine; IBM Research-Zürich, Rüschlikon, Switzerland

Thermal Considerations for Monolithic Integration of Three-Dimensional Integrated Circuits  104
A.K. Hemming1, B. Rajendran2, B. Cronquist1 and Z. Or-Bach1; 1Monolithic 3D, Inc. 2Department of Electrical Engineering, IIT-Bombay, Bombay, India

Concurrent Design Analysis of A 8500V ESD-Protected SP10T Switch in SOI CMOS  106
X.S. Wang1, X. Wang2, Z. Dong3, F. Lu1, L. Wang4, R. Ma1, C. Zhang3, A. Wang3, C.P. Yue4, D. Wang5 and A. Joseph6; 1Department of ECE, University of California, Santa Barbara, 2OmniVision Technologies, 3Department of EE, University of California, Riverside, 4Hong Kong University of Science and Technology, 5IBM Microelectronics

NW-TFET Analog Performance for Different Ge Source  108
P.G.D. Agopian1,2, S. D. dos Santos1, F.S. Neves1, J.A. Martino1, A. Vandooren2, R. Rooyackers3, E. Simoen1 and C. Claeys1,4; 1LSI/PSI/USP, University of Sao Paulo, Sao Paulo, Brazil, 2Centro Universitario da FEI, S.B. Campo, Brazil, 3Imec, Leuven, Belgium, 4E.E. Dept, KU Leuven, Leuven, Belgium

Dual Threshold Voltage Adder for Robust Sub-Vt Operation in 65nm Technology  110
M. Jagasivamani, M. Bajura, M. Fritze; Information Sciences Institute University of Southern California, Arlington, USA

Analysis of Vth Flexibility in Ultrathin-BOX SOI FinFETs  112
K. Endo, Y. Ishikawa, Y. Liu, T. Matsukawa, S. O’uchi, J. Tsukada, S. Migita, W. Mizubayashi, Y. Morita, H. Ota, H. Yamauchi, M. Masahara; Advanced Industrial Science and Technology (AIST), Tsukuba Ibaraki, Japan

SESSION 8a  SOI Memory

SESSION CHAIRS
Yuh-Yue Chen, Skyworks
Joao Antonio Martino,
University of São Paulo

The Evolution of Embedded Memory in High Performance Systems  N/A
S. Iyer; IBM (invited talk)

Charge Trapping Type FinFET Flash Memory with Al2O3 Blocking Layer  114
Y.X. Liu1, T. Nabatame2, T. Matsukawa4, K. Endo1, S. O’uchi2, J. Tsukada1, H. Yamauchi2, Y. Ishikawa3, W. Mizubayashi1, Y. Morita1, S. Migita1, H. Ota3, T. Chikyow2 and M. Masahara1; 1National Institute of Advanced Industrial Science and Technology (AIST), 2NIMS

GaP Source-Drain SOI 1T-DRAM: Solving the Key Technological Challenges  116
A. Pal1, A. Nainani2, Z. Ye2, X. Bao2, E. Sanchez2 and K.C. Saraswat1; 1Center of Integrated Systems, Stanford University, Stanford, USA, 2Applied Materials, Sunnyvale, CA
8a.4 Suppression of Self-Heating Effect Employing Bulk Vertical-Channel Bipolar Junction Transistor (BJT) Type Capacitorless 1T-DRAM Cell 118
T. Imamoto1,2 and T. Endoh1,2; 1Graduate School of Engineering, Tohoku University, Sendai, Japan, 2JST-CREST

8a.5 An Ultra-Fast Floating-Body/Gate Cell for Embedded DRAM 120
Z. Lu, J.G. Fossum, D. Sarkar and Z. Zhou; University of Florida, Gainesville, USA

SESSION 8b  Sub-Vt Microcontrollers and Memory

8b.1 V_{min}=0.4 V LSIs are the Real with Silicon-on-Thin-Buried-Oxide (SOTB) - How is the Application with "Perpetuum-Mobile" Micro-controller with SOTB? 122
N. Sugii1, T. Iwamatsu1, Y. Yamamoto1, H. Makiyama1, H. Shinohara1, H. Oda1, S. Kamohara1, Y. Yamaguchi1, K. Ishibashi2, T. Mizutani1, T. Hiramoto1
1Low-power Electronics Association & Project (LEAP), Ibaraki, Japan, 2The University of Electro-Communications, Tokyo, Japan, 3Institute of Industrial Science, The University of Tokyo, Tokyo, Japan (invited talk)

8b.2 An Ultra Low Energy 9T Half-select-free Subthreshold SRAM bitcell 124
A. Banerjee and B.H. Calhoun; University of Virginia, Charlottesville, Charlottesville, USA

8b.3 0.42-to-1.20V Read Assist Circuit for SRAMs in CMOS 65nm 126
F. Abouzeid, S. Clerc, B. Pelloux-Prayer and P. Roche; STMicroelectronics, Crolles, France

8b.4 A 13T Radiation Hardened SRAM Bitcell for Low-Voltage Operation 128
L. Atias1, A. Teman1 and A. Fish2; 1VLSI Systems Center, Ben-Gurion University of the Negev, Be'er Sheva, Israel, 2Faculty of Engineering, Bar-Ilan university, Ramat Gan, Israel

8b.5 SRAM Row Decoder Design for Wide Voltage Range in 28nm UTBB-FDSOI 130
G. Suraci, B. Giraud, T. Benoist, A. Makosiej, O. Thomas; CEA-LETI, MINATEC, Grenoble, France

SESSION 9a Novel SOI Devices

9a.1 Ultra-Thin Body MOS Device Technologies Using High Mobility Channel Materials 132
S. Takagi, S.-H. Kim, M. Yokoyama, W.-K. Kim, R. Zhang and M. Takenaka; The University of Tokyo, Tokyo, Japan (invited talk)

9a.2 SOI and Engineered-SOI, Ideal Platforms for Building MEMS 134
F. Assaderaghi; InvenSense, San Jose, USA (invited talk)

9a.3 New Observation on Gate-Induced Drain Leakage in Silicon Nanowire Transistors with Epi-Free CMOS Compatible Technology on SOI Substrate 136
J. Fan, M. Li, X. Xu and R. Huang; Institute of Microelectronics, Peking University, Beijing, China
9a.4  **Back Bias Influence on Analog Performance of pTFET**  138
P.G.D. Agopian1,2, F.S. Neves1, J.A. Martino1, A. Vandooren1, R. Rooyackers1, E. Simone3,4 and C. Claeyss3,4; 1LSI/PSI/USP, University of São Paulo, São Paulo, Brazil, 2Centro Universitário da FEI, São Bernardo do Campo, Brazil, 3imec, Leuven, Belgium, 4E.E. Department, KU Leuven, Leuven, Belgium

**SESSION 9b  Sub Vt – Devices**

**SESSION CHAIR**
Lew Cohn, NRO

9b.1  **New Directions in Analog to Digital Conversion**  N/A
M. Flynn; University of Michigan (invited talk)

9b.2  **Global Variability of UTBB MOSFET in Subthreshold**  140
S. Makovejev1, B.Kazemi Esfeh1, F. Andreiet1, J.-P. Raskin1, D. Flandre1, V. Kilchytska1; 1ICTEAM Institute, Université catholique de Louvain, Louvain-la-Neuve, Belgium, 2CEA-LETI, MINATEC Grenoble, France

9b.3  **A 44μW/10MHz Minimum Power Operation of 50K Logic Gate using 65nm SOTB Devices with Back Gate Control**  142
S. Morohashi1, N. Sugii2, T. Iwamatsu2, S. Kamohara2, Y. Kato1, C.-K. Pham1 and K. Ishibashi1; 1The University of Electro Communications, 2Low-Power Electronics Association & Project

9b.4  **Low Voltage, Steep Subthreshold, Beyond CMOS Technology**  N/A
A. Seabaugh; Notre Dame, (invited talk)

**SESSION 10  Hot Topics: 3DI**

**SESSION CHAIR**
Subu Iyer, IBM

10.1  **3D Integration of High Mobility InGaAs nFETs and Ge pFETs for Ultra Low Power and High Performance CMOS**  144
T. Irisawa1, M. Oda1, Y. Kamimuta1, Y. Moriyama1, K. Ikeda1, E. Mieda1, W. Jevasuwan1, T. Maeda1, O. Ichikawa2, T. Osada2, M. Hata2, and T. Tezuka1; Collaborative Research Team Green Nanoelectronics Center (GNC), AIST, Tsukuba, Japan, Sumitomo Chemical Co. Ltd, Tsukuba, Japan (invited talk)

10.2  **3D-Enabled Heterogeneous Integrated Circuits**  146

10.3  **Three-Dimensional Wafer Stacking using Cu TSV integrated with 45nm high performance SOI-CMOS embedded DRAM technology**  175
P. Batra1, D. LaTulipe2, S. Skordas2, K. Winstel2, C. Kothandaraman1, B. Himmel1, G. Maier1, B. He1, D. W. Gamage1, J. Golz1, W. Lin1, T. Vo1, D. Priyadarshini2, A. Hubbard2, K. Cauffman2, B. Peethala2, J. Barth1, T. Kiriha1, T. Graves-Abe1, N. Robson1, S. Iyer1; IBM Corporation Systems and Technology Group, 1Hopewell Junction, USA, 2Albany, USA, 3Burlington, USA (invited talk)
10.4 **3D Hetero-Integration Technology with Backside TSV and Reliability Challenges**  
K.-W. Lee, M. Murugesan, T. Fukushima, T. Tanaka and M. Koyanagi; *Tohoku University (invited talk)*

10.5 **Fine Grained 3D Cache Architecture Using High Density TSVs**  
I. Miro-Pandes; *CEA-Leti, Grenoble, France (invited talk)*

---

**SESSION 11**  
**LATE NEWS**

**SESSION CHAIR**  
Jean-Luc Pellioe, ARM

11.1 **SOI Lateral Bipolar Transistor with Drive Current >3mA/μm**  
J. Cai, T.H. Ning, C.D’Emic, J.-B. Yau, K. K. Chan, J. Yoon, K. A. Jenkins, R. Muralidhar and D.-G. Park; *IBM Research Division, Yorktown Heights*

11.2 **Three-Dimensional Integrated Circuits with NFET and PFET on Separate Layers Fabricated by Low Temperature Au/SiO2 Hybrid Bonding**  
M. Goto1, K. Hagiwara1, Y. Iguchi1, H. Ohtake1, T. Saraya2, E. Higurashi2, H. Toshiyoshi2, and T. Hiramoto2; 1NHK Science and Technology Research Laboratories, Tokyo, Japan, 2 The University of Tokyo, Tokyo, Japan

11.3 **Aggressively Scaled Strained Silicon Directly on Insulator (SSDOI) FinFETs**  
A. Khakifirooz1, R. Sreenivasan1, B.N. Taber1, F. Allibert2, P. Hashemi3, W. Chern4, N. Xu3, E.C. Wall1, S. Mochizuki1, J. Li1, Y. Yin3, N. Loubet1, A. Reznicek1, S.M. Mignot3, D. Lu1, H. He1, T. Yamashita1, P. Morin3, G. Tsutsui1, C.-Y. Chen1, V.S. Basker1, T.E. Standaert1, K. Cheng1, T. Levin1, B.Y. Nguyen2, T.-S. King Liu3, D. Guo1, H. Bu1, K. Rim1, and B. Doris1; 1IBM, 2SOITEC, 3STMicroelectronics, Albany, USA, 4MIT, Cambridge, USA, 5University of California, Berkeley, USA