46th International Symposium on Microelectronics

(IMAPS 2013)

**Orlando, Florida, USA
30 September - 3 October 2013**

ISBN: 978-1-62993-824-0

Printed from e-media with permission by:

Curran Associates, Inc.
57 Morehouse Lane
Red Hook, NY 12571

Some format issues inherent in the e-media version may also appear in this print version.

Copyright© (2013) by IMAPS - International Microelectronics & Packaging Society
All rights reserved.

Printed by Curran Associates, Inc. (2014)

For permission requests, please contact
IMAPS - International Microelectronics & Packaging Society
at the address below.

IMAPS - International Microelectronics & Packaging Society
611 2nd St, NE
Washington, DC 20002

Phone: (202) 548-4001
Fax: (202) 548-6115

imaps@imaps.org

Additional copies of this publication are available from:

Curran Associates, Inc.
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: 845-758-0400
Fax: 845-758-2634
Email: curran@proceedings.com
Web: www.proceedings.com

TABLE OF CONTENTS

TSV MATERIALS & PROCESSES

FEATURED: Alternative Technology Concepts for Low-Cost and High-Speed 2D and 3D Interconnect Manufacturing	1
<i>Fred Roozeboom, M. Smets, B. Kniknie, H. Hoppenbrouwers, G. Dingemans, W. Keuning, W. M. M. Kessels, R. Pohl, A. J. Huis In'T Veld</i>	
ABSTRACT: Optimizing TSV Liner Step Coverage	7
<i>Vijayalakshmi Seshachalam</i>	
Monitoring of Wet Etch for Wafer Thinning and Via Reveal Process.....	8
<i>Eugene Shalyt, Eugene Shalyt, Guang Liang, Peter Bratin</i>	
2.5/3D Packaging Technology Solution for High Frequency Device	13
<i>Yasuhiro Morikawa, Takahide Murayama, Toshiyuki Sakuishi, Koukou Suu</i>	
Application of Low-K Liner for Stress and Capacitance Control in Cu-TSV	17
<i>Chuan Seng Tan, L. Zhang, H. Y. Li, W. Yoo</i>	
Electrografted Insulator Layer as Copper Diffusion Barrier for TSV Interposers.....	22
<i>Vincent Mevellec, F. Raynal, D. Suhr, T. Dequivre, L. Religieux</i>	
Analysis of Stress/Strain in Electroless Copper Films.....	26
<i>Tobias Bernhard, Simon Bamberg, Frank Bruning, Ralf Bruning, Laurence J. Gregoriades, Tanu Sharma, Delilah Brown, M. Klaus, Ch. Genzel</i>	

DESIGN & ANALYSIS FOR RELIABILITY

Using Physics of Failure to Predict System Level Reliability for Avionic Electronics	31
<i>Greg Caswell</i>	
Solder Joint Reliability Study for Wafer Level Packages on Flexible and Rigid Boards	39
<i>Gary Gu, Jon Chadwick, Daniel Jin</i>	
Ag Wire and Ag Alloy Wire Reliability and Molding Compounds	45
<i>Aya Mizushima, Shinichiro Kato, Hidenori Abe, Naoki Sadayori, Yoshinori Endo</i>	
Moisture Reliability Improvement of a High Performance Depletion Mode 0.15um Gate PHEMT Process	50
<i>Jon Abrokwhah, John Stanback, Jerry Wang, Molly Johnson, Chi L. Jiaa</i>	
LORD SolderBrace (TM) Wafer Applied Coating for Improved Reliability and Throughput in WLCSP	55
<i>George Sears, Guoyun Tian, Duy Le, Heather Bradley</i>	
Moisture and Hydrogen Release in Optoelectronic Hermetic Packages	61
<i>Marwan Aalbahghouti, N. El Dahbah, G. Perosevic, S. Jain, J. M. Papillon, S. Fernandez</i>	

ADVANCED MATERIALS & NOVEL ASSEMBLY PROCESSES

Development of Laser and Photodefinable Toughened Benzocyclobutene Dielectric Materials for 3D-TSV Integration	67
<i>Zidong Wang, Michael Gallagher, Kevin Wang, Elissei Iagodkine, Mark Oliver, Joe Lachowski, Greg Prokopowicz, Eric Huenger, Raymond Thibault, Zhifeng Bai, Christopher Tucker, Matthew Bishop, Scott Kisting, Lynne Mills, David Louks</i>	
Small-Chip Attachment on Copper Leadframe with Sintered Nanosilver Paste	72
<i>Jesus Calata, Hanguang Zheng, Guo-Quan Lu, Khai Ngo</i>	
Influence of the Organic Vehicle and Inorganice Additives on the Properties of Thick Film Pastes for AlN.....	78
<i>Richard Schmidt, Marco Wenzel, Kathrin Reinhardt, Uwe Partsch, Lars Rebenklau, Markus Eberstein</i>	
Better, Faster and Cheaper Precision Cleaning: Advanced CO₂ Cleaning Technology	84
<i>David Jackson</i>	
Copper Wirebond Compatibility with Organic and Inorganic Ions Present in Mold Compounds.....	89
<i>Varughese Mathew, Sheila Chopin, Leo Higgins, Yingrui Zhang</i>	
A Non-Through Silicon Via 1000+ IO Package on Package Solution for Wide IO Applications.....	94
<i>Laura Mirkarimi, Rajesh Katkar, Ron Zhang, Rey Co, Zhijun Zhao</i>	

PB-FREE SOLDER & ROHS

Effects of Minor Alloying Additive on the Shear Strength of Sn-58Bi Solder Joint.....	100
<i>Omid Mokhtari, Hiroshi Nishikawa</i>	
Effects of Sb and Zn Addition on Impact Resistance Improvement of Sn-Bi Solder Joints.....	104
<i>Keishiro Okamoto, Kenji Nomura, Shuichi Doi, Toshiya Akamatsu, Seiki Sakuyama, Keisuke Uenishi</i>	
Effect of Fe Content on the Interfacial Reliability of SnAgCu/Fe-Ni Solder Joint	109
<i>Hao Zhang, Qing-Sheng Zhu, Zhi-Quan Liu, Li Zhang, Hongyan Guo, Chi-Ming Lai</i>	
Effect of ENEPIG Surface Finish on the Vibration Reliability of Solder Interconnects.....	115
<i>Sandeep Menon, Adam Pearl, Michael Osterman, Michael Pecht</i>	

Thermal Cycling Reliability of Alternative Low-Silver Tin-based Solders	120
<i>Elviz George, Michael Osterman, Michael Pecht, Richard Coyle, Richard Parker, Elizabeth Benedetto</i>	
Voiding and Reliability of Assembly of BGA with SAC and 57Bi42Sn1Ag Alloys.....	128
<i>Ning-Cheng Lee, Yan Liu, Joanna Keck, Erin Page</i>	
Thermal Cycle Consideration in Applying Lead-Free TFBGA Simulation to a Design	140
<i>Yi-Chuan Tsai, Mei-Ling Wu</i>	

MEDICAL DEVICE PACKAGING

FEATURED: How are CCD, CMOS and A-Si Reshaping the Medical Imaging Industry?	147
<i>Christophe Fitamant</i>	
Biomedical Sensor Packaging Failures: Regulations are Not Design Standards	148
<i>Colin Drummond</i>	
Evaluation of Epoxy Flux for Use in Hearing Aid SMD Assemblies	152
<i>Susie Johansson, John Dzarnoski</i>	
Anti-Counterfeit, Advanced Microelectronics Packaging Solutions for Miniaturized Medical Devices.....	158
<i>Rabindra Das, Frank D. Egitto, How Lin</i>	
Non-Hermetic Micropackage for Chronic Implantable Systems.....	166
<i>P. Wang, S. B. Lachhman, D. Sun, S. J. A. Majerus, M. S. Damaser, C. A. Zorman, P. X. L. Feng, W. H. Ko</i>	

EUROPEAN PERSPECTIVE ON PACKAGING TRENDS

FEATURED: Assembly and Packaging Enabling System Integration	171
<i>Klaus Pressel, Gottfried Beer, Maciej Wojnowski</i>	
Smart Power Module Molding Advances: Evaluating High Temperature Suitability of Molding Compounds.....	177
<i>K.-F. Becker, T. Thomas, J. Bauer, R. Kahle, T. Braun, R. Aschenbrenner, M. Schneider-Ramelow, K. D. Lang</i>	
Ultrasonically Enabled Low Temperature Electroless Plating for Advanced Electronic Manufacture	183
<i>Andrew Cobley, J. E. Graves, A. Kassim, B. Mikhlef, B. Abbas</i>	
Hybrid In-Mould Integration.....	188
<i>Teemu Alajoki, Matti Koponen, Arttu Huttunen, Markus Tuomikoski, Mikko Heikkinen, Antti Keranen, Kimmo Karenen, Jukka-Tapani Mäkinen, Tuomo Jaakola, Janne Aikio, Kari Ronka</i>	
Excimer Laser Machining of Fired LTCC for Selectively Metallized Open Channel Structures	194
<i>Dilshani Rathnayake-Arachchige, David A. Hutt, Paul P. Conway</i>	
An Overview of Isotropic Conductive Adhesives Filled with Metal-Coated Polymer Spheres	200
<i>Hoang-Vu Nguyen, Knut E. Aasmundveit, Helge Kristiansen, Tore Helland</i>	
A Friction Based Approach for Modeling Wire Bonding	208
<i>Simon Althoff, Jan Neuhaus, Tobias Hensel, Walter Sextro</i>	

STUDENT/UNIVERSITY POSTER SESSION

POSTER: Integrated ψ-Type Photonic Polarization Diversity Receivers for Wireless Radio-Over-Fiber Communication Links.....	213
<i>V. Rymanov, S. Dulme, M. Wachholz, M. Palandoken, T. Tekin, A. Stohr</i>	

ADVANCED PLATFORM INTEGRATION

Enabling a Manufacturable 3D Technologies and Ecosystem Using 28nm FPGA with Stack Silicon Interconnect Technology	217
<i>Woon-Seong Kwon, Myongseob Kim, Jonathan Chang, Suresh Ramalingam, Liam Madden, Genie Tsai, Stephen Tseng, J. Y. Lai, Terren Lu, Steve Chiu</i>	
DIMM-in-a-PACKAGE (DIAP) Signal Integrity for High-Performance on-Board Memory Applications.....	223
<i>Zhuowen Sun, Kevin Chen, Richard Crisp</i>	
High Speed Signal Transmission using Through-Si Vias and Coplanar Waveguides in a 3D IC Test Structure.....	228
<i>Min Xu, Robert Geer, Pavel Kabos, Thomas Wallis</i>	
ABSTRACT: Electrical Characterization of TSVs with Varying Process Knobs and Temporary Bond/Adhesive System Robustness Studies for 2.5D/3D Manufacturing	233
<i>Niranjana Kumar</i>	
ABSTRACT: Polymer Based Interposer Providing ESD and Thermal Robustness	234
<i>Karen Shrier</i>	

MODELING AND DESIGN FOR SI AND RELIABILITY

Flip-Chip Packages with Periphery Cu Pillar Bumps as Wire Bond Replacement - Design, Modeling & Characterization	235
<i>Zhe Li, Siow Chek Tan, Yee Huan Yew, Pheak Ti The, M. J. Lee, John Xie</i>	

Package Technology Selection of 28nm High Power FPGA with Pb-Free Solder Bumps: Flip Chip Molded BGA (FC^mBGA) Versus Traditional Flip Chip Bare Die Package	239
<i>Corey Reichman, Michael Lyakas, Miguel Jimarez, Romina Mimi Ocampo, Aaron Elberg, Altaf Hasan, Dierdre Hale, Fred Hamilton, Joon Dong Kim</i>	
Modeling and Reliability Analysis of TSVs for High Frequency Applications	245
<i>Kaushal Kannan, Bruce Kim, Sureshwar Kannan, Seok-Ho Noh</i>	
Design for Solder Joint Fatigue Life of BGA Package Subject to Mechanical Environment	250
<i>Mei-Ling Wu, Jia-Shen Lan</i>	
Warpage Characterization and Improvements for IC Packages with Coreless Substrate	260
<i>Bora Baloglu, Wei Lin, Ken Stratton, Miguel Jimarez, Danny Brady</i>	

POLYMERS, UNDERFILL, ENCAPSULANTS AND ADHESIVES

A Novel High Thermal Conductive Underfill for Flip Chip Application.....	265
<i>Wusheng Yin, Mary Liu</i>	
An Overview of Molded Underfill in Flip Chip Packaging Applications.....	271
<i>Fernando Roa</i>	
Packaging Materials for 2.5/3D Technology.....	276
<i>Brian Schmaltz</i>	
Thermo-mechanical Stress of Underfilled 3D IC Packaging.....	285
<i>Ming-Han Wang, Mei-Ling Wu</i>	
Solder Joint Encapsulant Adhesive - LGA High Reliability and Low Cost Assembly Solution	291
<i>Wusheng Yin, Mary Liu</i>	
Adhesion and Cure Mechanism Studies for Advanced Lidded Flip Chip Applications	298
<i>Lyndon Larson, Kristen E. Steinbrecher</i>	

WIREBONDING & STUD BUMPING

Non-Destructive Top Layer Bond Pad Cross Section	303
<i>Terence Q. Collier, Indira Gubeljic</i>	
Stitch Bond Process of Pd-Coated Cu Wire: Experimental and Numerical Studies of Process Parameters and Materials.....	312
<i>A. Rezvani, M. Mayer, I. Qin, J. Brunner, Bob Chylak</i>	
Cu Heavy Wirebonding for High Power Device Interconnection.....	318
<i>Baik-Woo Lee, Chang-Sik Kim, Changmo Jeong, Younghun Byun, Jeong-Won Yoon, Che-Heung Kim, Seong Woon Booh</i>	
Multipurpose Wire Bonding - Bumps, Wires, Combination Interconnects, and Operation Efficiency.....	324
<i>Daniel Evans</i>	
Automated Wirepull Testing - Parallelogram of Forces-Real Time Applications	331
<i>Richard Garcia, Josef Sedlmair</i>	
Thick Copper and Aluminum Wire Bonding Technology for High Power Laser Devices	336
<i>Kong Weng Lee, Lei Xu, Jay Skidmore</i>	
Study of Wirebonding on Thin Al Pads with Various Size Probe Marks	341
<i>Shashi Sharma, Andrew Forhan, Prakash Subedi, Dustin Whittaker, Stevan Hunter</i>	
High Speed Aluminum Wirebonding for Molded Packages.....	347
<i>Luu Nguyen</i>	

EMERGING TECHNOLOGIES

DNA Marking: Implementation of a Proactive Counterfeit Risk Mitigation Solution	348
<i>Janice Meraglia</i>	
Transferable Redistribution Layers (TRDL).....	349
<i>David Herndon, Suzanne Dunphy</i>	
Implementing Inductor Function with Vibrating Capacitor Structures	354
<i>Thomas Marinis, Joseph W. Soucy</i>	
Embedded Photonics Interconnect Eco-System for Data Center Applications.....	361
<i>Richard Pitwon, Kai Wang, Alex Worrall</i>	
Decision Making Model for the Emerging Nanotechnologies	367
<i>Kewal Verma, Audre Dixon</i>	
Ultra-Thin Flexible Ceramic Membranes for Electronic Applications.....	379
<i>John Olenick</i>	
A Study on Prevalent Factors Behind Efficiency Deterioration of a Typical Low Power Solar Panel.....	384
<i>Virgil Ganescu, A. Pascu</i>	

ASIAN PERSPECTIVE ON ELECTRONIC PACKAGING AND SYSTEM INTEGRATION

FEATURED: Thin-Wafer Handling with a Heat-Spreader Wafer for 2.5D/3D IC Integration	389
<i>John Lau, H. C. Chien, S. T. Wu, Y. L. Chao, W. C. Lo, M. J. Kao</i>	

Electroless Ni Plating Solutions for Reproducible Black Pad Analyses	397
<i>Jin Yu, K. H. Kim</i>	
Scaling Challenges of Semiconductor Packaging in the Era of Big Data.....	402
<i>Yasumitsu Oriti, Akihiro Horibe, Kazushige Toriyama, Keiji Matsumoto, Hirokazu Noma, Sayuri Kohara, Toyohiro Aoki, Kuniaki Sueoka, Hiroyuki Mori</i>	
High Thermal Conductive Inter Chip Fill For 3D-IC Through Pre-Applied Joining Process.....	408
<i>Y. Kawase, M. Ikemoto, M. Yamazaki, M. Sugiyama, H. Kiritani, F. Mizutani, K. Matsumoto, A. Horibe, H. Mori, Y. Oriti</i>	
Development of Organic Multi Chip Package for High Performance Application	414
<i>Noriyoshi Shimizu, Wataru Kaneda, Hiromu Arisaka, Naoyuki Koizumi, Satoshi Sunohara, Akio Rokugawa, Toshimori Koyama</i>	
Thermally Activated Bumping Process using Sn3.0Ag0.5Cu Solder Powder for Low-Cost Interposers	420
<i>Kwang-Seong Choi, Ho-Eun Bae, Haksun Lee, Hyun-Cheol Bae, Yong-Sung Eom</i>	
Low Temperature Si-Si, SiO₂-SiOs Covalent Bonding Structures with Thin Siloxane Layer	424
<i>Jeongyub Lee, Kunmo Chu, Yongyoung Park, Wooyoung Yang, Wenxu Xianyu, Changyoul Moon</i>	

PACKAGING TRANSITIONS: 2.5D AND 3D INTERCONNECT TECHNOLOGIES FROM WIRE BOND TO RDL TO TSV

Cost Comparison of 2.5D/3D Packaging to Other Packaging Technologies.....	429
<i>Chet Palesko, Amy Palesko, E. Jan Vardaman</i>	
Redistribution Layers (RDLs) for 2.5D/3D IC Integration	434
<i>John Lau, P. Tzeng, C. Lee, C. Zhan, M. Li, J. Cline, K. Saito, Y. Hsin, P. Chang, J. Chen, S. Chen, C. Wu, H. Chang, C. Chien, C. Lin, T. Ku, R. Lo, M. Kao</i>	
A Wide I/O Memory-on-Logic Product Prototype Enabled by Through-Silicon Stacking Technology	442
<i>Vidhya Ramachandran, Dong Wook Kim, Sam Gu, Ron Lindley, Brian Henderson, Urmi Ray, Riko Radojcic, Matt Nowak, Aurel Gunterus, Amer Cassier</i>	
3D RCP Packaging Stacking: Side Connect, an Emerging Technology for System Integration and Volumetric Efficiency	447
<i>Michael Vincent, Doug Mitchell, Jason Wright, Yap Weng Foong, Alan Magnus, Zhiwei Gong, Scott Hayes, Navjot Chhabra</i>	
3D Integrated Packaging Approach for High Performance Processor - Memory Module.....	452
<i>Stephen Polzer, W. L. Wilkins, J. L. Fasig, M. J. Degerstrom, B. K. Gilbert, E. S. Daniel</i>	
Next-Generation Lead-Free Solder Plating Products for High Speed Bumping, Capping and Micro-Capping Applications.....	458
<i>Jonathan Prange, Julia Woerting, Yi Qin, Pedro Lopez Montesinos, Inho Lee, Yil-Hak Lee, Masaaki Imanari, Jianwei Dong, Jeffrey Calvert</i>	

THERMAL AND THERMO-MECHANICAL MODELING

Interactions between Variable Frequency Microwave Undefill Processing and High Performance Packaging Materials.....	461
<i>Mamadou Diobet Diop, Marie-Claude Paquet, Dominique Drouin, David Danovitch</i>	
Heat Sink Induced Thermo-Mechanical Joint Strain in QFN Devices	467
<i>Gerard McVicker, Vijay Khanna, Sri M. Sri-Jayantha</i>	
Fatigue Life Analysis of Sn96.5Ag3.0Cu0.5 Solder Thermal Interface Material of a Chip-Heat Sink Assembly in Microelectronic Applications	473
<i>M. Ekpu, R. Bhatti, M. I. Okereke, K. C. Otiaba</i>	
Thermally and Electrically Enhanced Wirebond BGA	478
<i>Burton Carpenter, Leo M. Higgins III, Robert Wenzel, Boon Yew Low, Sriram Neelakantan, Daniel Boyne</i>	
ABSTRACT: Accurate Finite Element Analysis of Embedded Wafer Level Packaging by Thermomechanical Characterization of Materials and ICs Piezoresistive Stress Sensors.....	484
<i>Sinh Vuhoang</i>	
ABSTRACT: Evaluation of Thermal Performance for a new Ventilated Heat Sink Module.....	485
<i>Shiang-Jiun Lin</i>	

SUBSTRATE MATERIALS I

Effects of Copper Pattern Density and Orientation on the Modulus of BGA Substrates.....	486
<i>Burton Carpenter, Betty Yeung, Yuan Yuan</i>	
A Photo-Desmear Method for Via Residue Removal Using at VUV Light Source.....	492
<i>Tomoyuki Habu, Shintaro Yabu, Kenichi Hirose, Hiroki Horibe, Toru Fujinami, Naoki Kitano, Eiji Ozawa</i>	
Method to Measure Effects of Surface Roughness on High-Frequency Transmission Lines.....	496
<i>Toshiki Iwai, Daisuke Mizutani, Motoaki Tani</i>	
Analysis of the Thick Film Deposited on Alumina Substrate and Effect of Different Parameters on the Response of Propanol Using Taguchi Method	500
<i>Ibrahim Gaidan</i>	
RF Capacitor Material for Use in Printed Circuit Board.....	507
<i>Jin-Hyun Hwang, John Andresakis, Ethan Feinberg, Bob Carter, Yuji Kageyama, Fujio Kuwako</i>	

Characterization of CVD Diamond for Thermal Management Applications	511
<i>R. S. Balmer, B. Bolliger, J. M. Dodson, D. J. Twitchen</i>	

FLIP CHIP BUMPING

Development of an Ultra Thin Die-to-Wafer Flip Chip Stacking Process for 2.5D Integration	516
<i>Gabriel Pares, A. Attard, F. Dosseul, A. N'Hari, O. Boillon, L. Toffanin, G. Klug, G. Simon</i>	
Long-term Electromigration Study of Lead-Free Flip-Chips with Solder Bumps with 50 µm or 60 µm Diameter Employing ENIG Surface Finish on Both Chip and Substrate Side	523
<i>Marek Gorywoda, Rainer Dohle, Stefan Harter, Andreas Wirth, Jorg Gobler, Jorg Franke</i>	
3D Integration of System-in-Package (SiP) Using Organic Interposer: Toward SiP-Interposer-SiP for High-end Electronics	531
<i>Rabindra Das, Frank D. Egitto, Steven G. Rosser, Erich Kopp, Barry Bonitz, Raj Rai</i>	
Organic Chip Scale Package (CSP) Development for Flip Chip Applications	538
<i>Tomoyuki Yamada, Masahiro Fukui, Kenji Terada, Masaaki Harazono, Teruya Fujisaki, Charles Reynolds, Jean Audet, Yi Pan, Scott Moore, Sushumna Iruvanti</i>	
Improving WLCSP Reliability Through Solder Joint Geometry Optimization	546
<i>Boyd Rogers, Chris Scanlan</i>	
ABSTRACT: Isothermal Fatigue Tests on Sn63-Pb37, Sn62-Pb36-Ag2 and Sn42-Bi58 Solder Joints.....	551
<i>Eliane Grigoletto</i>	

NEW CONCEPTS, INTERCONNECTS & PROCESSES FOR HIGH PERFORMANCE PACKAGING

Si Vapor Chamber Integrated with Through Silicon Via for 3D Packaging.....	552
<i>Jun Taniguchi, Takeshi Shioga, Yoshihiro Mizuno</i>	
Inspection and Metrology Solutions from TSV through Reveal for High Volume Manufacturing.....	558
<i>Rajiv Roy, Russ Dudley, David Marx, David Grant, Matt Wilson, Scott Balak</i>	
Multi Beam Low-k Grooving Evaluation of Various Removal Principals.....	564
<i>Jeroen Van Borkulo, Richard Van Der Stam, Peter Dijkstra</i>	
Stencil Printing Process Guidelines for 0.3mm Pitch Chip Scale Packages.....	569
<i>Mark Whitmore, Jeff Schake, Clive Ashmore</i>	
Z-Axis Interconnection: A Versatile Technology Solution for High Performance Electronics.....	574
<i>Rabindra Das, John M. Lauffer, Frank D. Egitto</i>	

POWER PACKAGING I

ABSTRACT: Energy Efficient Electronics: An Objective, a Resource, a Market	582
<i>Jeff Perkins</i>	
The Next Level of Accurate Server Power Monitoring and Capping.....	583
<i>Jerry Steele</i>	
Package Design and Development of a Low Cost High Temperature (250°C), High Current (50+A), Low Inductance Discrete Power Package for Advanced Silicon Carbide (SiC) and Gallium Nitride (GaN) Devices	592
<i>Brice McPherson, B. Passmore, P. Killeen, D. Martin, A. Barkley, T. McNutt</i>	
Advanced Thermal Simulation Model for Power MOSFETs	598
<i>Jens Ejury</i>	
A Highly Integrated GaAs-based Module for DC-DC Regulators	604
<i>Greg Miller</i>	

GLASS INTERPOSERS

Thermal Characteristic and Performance of the Glass Interposer with TGVs (Through-Glass Via).....	611
<i>Heng-Chieh Chien, Chun-Hsien Chien, Ming-Ji Dai, Ra-Min Tain, Wei-Chung Lo, Yung-Jean Rachel Lu</i>	
Performance and Process Comparison between Glass and Si Interposer for 3D-IC Integration	618
<i>Chun-Hsien Chien, Ching-Kuan Lee, Hsun Yu, Chang-Chih Liu, Peng-Shu Chen, Heng-Chieh Chien, Jen-Hau Cheng, Li-Ling Liao, Ming-Ji Dai, Yu-Min Lin, Chau-Jie Zhan, Cheng-Ta Ko, Wei-Chung Lo, Yung Jean Lu</i>	
Glass Interposer Substrates: Fabrication, Characterization and Modeling.....	625
<i>Aric Shorey, Satish Chaparala, Scott Pollard, Garrett Piech, John Keech</i>	
Development of TGV Interposer for 3D IC.....	631
<i>Shintaro Takahashi, Kentaro Tatsukoshi, Motoshi Ono, Masaki Mikayama, Nobuhiko Imajo</i>	
Challenges of Adhesion Promotion for the Metallization of Glass Interposers.....	635
<i>Robin Taylor, Simon Bamberg, Michael Mersch, Tobias Bernhard, Frank Bruening, Lutz Brandt, Zhiming Liu, Hailuo Fu, Sara Hunegnaw</i>	

TESTING METHODS AND PROCESS FOR IMPROVED RELIABILITY

Advanced Warpage Characterization for FOWLP	641
<i>Isabel Barros, Mario Ribeiro, Nelson Pinho, S. A. Naniun</i>	

An Analysis of Evolving Package Reliability Test Methodologies for Wireless Applications	647
<i>Michael Ferrara</i>	
The Effectiveness of Screening Techniques for Revealing Cracks in High Volumetric Efficiency MLCCs.....	651
<i>Alexander Teverovsky</i>	
Dicing Development for Low-k Copper Wafers using Nickel-Palladium-Gold Bond Pads for Automotive Application	657
<i>Tu Anh Tran, Varughese Mathew, Wen Shi Koh, K. Y. Yow, Y. K. Au</i>	
Immersion Tin for QFN Packages to Create a 3-D Solder Joint for Reliability Enhancement.....	663
<i>Mustafa Oezkoek</i>	
A Fully Automated Execution of Complex DOE to Characterize Electroplating Baths	667
<i>Norbert Schroeder, Fred Richter, Juerg Stahl, Arnold Cziurlok</i>	
Improvement of Back-Side Cosmetic Defects and Wafer Strength	672
<i>Victoria L. Calero-Ddelc, Irene Popova, Aaron Bicknell, Richard Indyk, Joe Sullivan, John Fitzsimmons</i>	

SUBSTRATE MATERIALS II (CERAMIC & LTCC)

Plating Reliability and High Frequency Testing of DuPont™ GreenTape™ 9K7 LTCC	678
<i>Allan Beikmohamadi, Patricia Graddy, Deepukumar Nair, Jim Parisi, Steve Stewart</i>	
A Low Loss Power Distribution Network Design in Low Temperature Co-Fired Ceramic Technology	683
<i>Michael Glover, Michael C. Hamilton, Emmanuel Decrossas, Kaoru Porter, Alexander Pfeiffenberger, H. Alan Mantooth</i>	
Thick Film Pastes for Nitride Ceramics for High Power Applications	689
<i>Marco Wenzel, Richard Schmidt, Uwe Partsch, Markus Eberstein</i>	
Low-Temperature Co-Fired Ceramic (LTCC) Technology for Development of Sensors for Emerging Applications.....	695
<i>Hansu Birol, S. Lopera, G. Farine, T. Maeder, W. B. Quintao, J. Gervasio, E. Gyoervary, L. O. S. Cesar, J. Buntaine, P. Ryser</i>	

MEMS & SENSOR PACKAGING

A Current-Controlled PCB Integrated MEMS Tilt Mirror	700
<i>Robert Dean, Colin B. Stevens, John J. Tatarchuk</i>	
High and Moderate-Level Vacuum Packaging of Vibratory MEMS	705
<i>Igor Prikhodko, Brenton R. Simon, Gunjana Sharma, Sergei A. Zotov, Alexander A. Trusov, Andrei M. Shkel</i>	
Microfluidic Device Packaging	711
<i>Leland "chip" Spangler</i>	
Void Formation and Bond Strength Investigated for Wafer-level Cu-Sn Slid Bonding	717
<i>Astrid-Sofie Vardoy, H. J. Van De Wiel, Stian Martinsen, Greg R. Hayes, Hartmut R. Fischer, Knut E. Aasmundtveit, Adriana Lapadatu, Maaiké M. V. Taklo</i>	
Mechanical Stress Analyses of Packaged Pressure Sensors for Very High Temperatures	723
<i>Roderich Zeiser, Suleman Ayub, Jochen Hempel, Michael Berndt, Juergen Wilde</i>	
ABSTRACT: Packaging CMUTs for Gesture Sensing	729
<i>Luu Nguyen</i>	

THINK THIN: THIN IC PACKAGING FOR MOBILE DEVICES

Active and Passive Component Embedding into Low-Cost Plastic Substrates Aimed at Smart System Applications	730
<i>Maarten Cauwe, Bjorn Vandecasteele, Johan De Baets, Jeroen Van Den Brand, Roel Kusters, Ashok Sridhar</i>	
Modular Microsystems with Embedded Components	735
<i>Christian Boehme, Andreas Ostmann, Martin Schneider-Ramelow</i>	
Size Matters - Embedding as an Enabler of Next-Generation SiPs	740
<i>Nick Renaud-Bezot</i>	
ABSTRACT: Novel Back-Side Grinding and Laser Dicing Process for Cu Pillar Generated Low-K Wafer	745
<i>Yuka Tamadate</i>	
ABSTRACT: High Bandwidth PoP	746
<i>Jason Cho</i>	
ABSTRACT: Thin PoP for Mobile Devices - Conquering Technological and Process Challenges to Meet Customer Demands	747
<i>Sachin Deo</i>	
Compression Molding Solutions for Various High End Package and Cost Savings for Standard Package Applications.....	748
<i>Muneo Miura</i>	
ABSTRACT: Reducing Package Thickness to Accommodate Next Generation Smartphone Designs.....	752
<i>Brian Roggeman</i>	

POWER PACKAGING II

Electromigration in Lead - Free Solder: A Power IC Perspective.....	753
<i>Thomas Wassick</i>	
Conceptual Development Using 3D Printing Technologies for 8kV SiC Power Module Package	758
<i>Haotao Ke, Yang Xu, Douglas C. Hopkins</i>	

Improving System Performance with eGaN ® FETs in DC-DC Applications	764
<i>David Reusch, Johan Strydom, Alex Lidow</i>	
Source-Sense Packages for HV MOSFETs.....	770
<i>Anders Lind</i>	
Integrated Current Sensing Technology for Synchronous Buck Converters	776
<i>Evan Reutzel, Rengang Chen, Scott Ragona, David Jauregui</i>	
Detailed Analysis of How Power Stage and Power Clip Products Achieve Optimized Power Density	782
<i>Arthur Black</i>	

TECHNOLOGIES AND METHODS FOR 2.5/3D PACKAGING AND INTEGRATION

Lithography Process Optimization for 3D and 2.5D Applications	790
<i>Doug Shelton, Tomii Kume</i>	
Integrated Passive Devices and TSV, a Disputive Technology for Miniaturization	794
<i>Catherine Bunel, J. R. Tenaillon, F. Voiron S. Borel, A. Lefevre</i>	
"Front-end-ization" of the Back-End	799
<i>Rajiv Roy</i>	
Stacking of Known Good Rebuilt Wafers for High Performance Memory and SiP	804
<i>Pascal Couderc, Jerome Noiray, Christian Val</i>	
A Study on the Effectiveness of Underfills in the High Bandwidth Memory with TSV	810
<i>Woong-Sun Lee, Dae-Woong Lee, Ho-Young Son, Jin-Su Lee, Min-Suk Suh, Nick Kim, Kwang-Yoo Byun</i>	
Improved Compensation for a Reduction Stepper to Meet the Challenges for Advanced Packaging Applications	814
<i>James Webb, Steven Gardner, Elvino Dasilveira</i>	

RF AND MICROWAVE PACKAGING

Chip Design of an 1V RF Receiver Front-End for 5.8-GHz DSRC Applications	820
<i>Jhin-Fang Huang, Wen Cheng Lai, Yong-Jhen Jiangn</i>	
RF Device Integration on Glass Interposer Toward 3D-IPAC Packages	825
<i>Yoichiro Sato, Bruce Chou, Vijay Sukumaran, Junki Min, Motoshi Ono, Choikri Karoui, Franck Dosseul, Christian Nopper, Madhavan Swaminathan, Venky Sundaram, Rao Tummala</i>	
RF MEMS DPDT Switch Using Novel Simulated Seesaw Design	831
<i>Mohammed Al-Amin, Sufian Yousef, Barry Morris</i>	

BONDING MATERIALS AND PROCESSES

Silver Oxalate: Towards a New Solder Material for Highly Dissipative Electronic Assemblies.....	836
<i>K. Kiryukhina, H. Le Trong, P. Tailhades, J. Lacaze, M. Gougeon, V. Baco, F. Courtade, S. Dareys, O. Vendier, L. Raynaud</i>	
Development of Low Temperature Sintered Nano Silver Pastes using MO Technology and Resin Reinforcing Technology	842
<i>Koji Sasaki, Noritsuka Mizumura</i>	
Five Layer Cu-Coated Zn/Al Clad Solder for Die Attachment.....	848
<i>Takuto Yamaguchi, Osamu Ikeda, Shohei Hata, Yuichi Oda, Kazuma Kuroki</i>	
A Novel Epoxy Flux On Solder Paste For Assembling Thermally Warped POP	853
<i>Ning-Cheng Lee, Ming Hu, Lee Kresge</i>	
Production Proven, High Precision Temporary Bond/De-Bond Process.....	861
<i>Blake Dronen, Aric Shorey, B. K. Wang, Leon Tsai</i>	
Droplet-on-Demand Inkjet-Filled Through-Silicon Vias (TSVs) as a Pathway to Cost-Efficient Chip Stacking	866
<i>Jacob Sadie, Niels Quack, Ming C. Wu, Vivek Subramanian</i>	
ABSTRACT: Microstructure and Fracture Property of Cu/In/Cu Joints in 3D Package	872
<i>Yanhong Tian</i>	

LED AND OPTOELECTRONICS PACKAGING

Packaging of 1.3 Tb/s Full Duplex Optical Interconnect	873
<i>Shuki Benjamin, Kobi Hashar, Stanislav Stepanov, Gideon Katz, Amir Geron, Michael Mesh</i>	
Preparation of a Wafer-Level Micro Polymer Lens Array with Improved Performance Using a Low Cost Glass Mold	878
<i>Jintang Shang, Mengying Ma, Shunjin Qin, Chunwei Zhang, Li Zhang, Dong Chen, Chiming Lai</i>	
Compact Photonic Package for High-Power E-Band (60-90 GHz) Photoreceiver Modules.....	883
<i>V. Rymanov, M. Palandoken, S. Dulme, T. Tekin, A. Stohr</i>	
A Solder Joint Reliability Model for the Philips Lumileds LUXEON Rebel LED Carrier Using Physics of Failure Methodology.....	887
<i>Greg Caswell, Rudi Hechfellner, Michiel Kruger, Tewe Heemstra, Nathan Blattau, Vikrant More</i>	
ABSTRACT: The Effects of Humidity and Temperature Aging Test on Flexible Packaging LED Module.....	893
<i>Chunjin Hang</i>	
Effect of Voiding in Solder Joints on Thermal Performance of the LED	895
<i>Jianbiao Pan</i>	

Transient Thermal Analysis as a Test Method for the Reliability Investigation of High Power LEDs During Temperature Cycle Tests	902
<i>Gordon Elger, Shri Vishnu Kandaswamy, Robert Derix, Jurgen Wilde</i>	

PRINTED ELECTRONICS & ADDITIVE MANUFACTURING

FEATURED: 3D Additive Construction Using Regolith	908
<i>Robert Mueller</i>	
A Switched-Line Phase Shifter Fabricated with Additive Manufacturing	909
<i>Jonathan O'Brien, Eduardo Rojas, Thomas M. Weller</i>	
Fully 3D Printed 2.4 GHz Bluetooth/Wi-Fi Antenna	914
<i>Paul Deffenbaugh, Kenneth Church, Josh Goldfarb, Xudong Chen</i>	
Multi-Layer PC Boards Fabricated using Aerosol-Jet Printing	921
<i>John Bolger, Leon Lantz, Rich Lewis, Rick Trudeau, Daniel Hines</i>	
Precision Patterned Thin Films without Photolithography: Additive Manufacturing of Printed Electronics	927
<i>Scott Lauer, Whitten Little, Thomas Ambrose, Jeff Conrad, Tim Cowen</i>	
Non-Contact Characterization of Printed Resistors	932
<i>Maria Cordoba-Erazo, Thomas M. Weller</i>	

ELECTRONIC PACKAGING FOR HARSH ENVIRONMENT APPLICATIONS

Advanced Devices and Electronic Packaging for Harsh Environment	937
<i>Aicha Elshabini, Fred Barlow, Sharmin Islam, Pin-Jen Wang</i>	
High Temperature Sintered Interconnects Formed by Transient Liquid Phase Sintering	951
<i>Patrick McCluskey, Hannes Greve</i>	
Modeling of Failure in Aluminum Alloy Braze for a High Temperature Thermoelectric Assembly	957
<i>Shams Arifeen, G. Potirniche, A. Elshabini, F. Barlow</i>	
Thermal Evaluation of High-Current Polyimide Rigid and Rigid-Flex Printed Wiring Board Trace Widths in a Vacuum	964
<i>Bennion Cannon, Frank Friedl, Gary Gisler</i>	
Author Index	