Monday, May 19, 2014

Session 1: Yield Enhancement
Successful Yield Ramp using Product Test, Scan and Memory Diagnosis Ar
Venkatesan Muthumalai; David Iverson; Aaron Sinnott; Nancy Bell; Rao Desineni; Ritesh Turakhia; Thomas Berndt

Tristate Inverter Array: A new test structure that compliments traditional SRAM arrays as a yield learning vehicle
Ishtiaq Ahsan; Carl Schiller; Zhigang Song; Robert Wong; David Clark; Felix Beaudoin; Fred Towler

Novel Process Window and Product Yield Improvement by Eliminating Contact Shorts An
Yuan-Chieh Chiu; Shih-Ping Hong; Fang-Hao Hsu; Hong-Ji Lee; Nan-Tzu Lian; Tahone Yang; Kuang-Chao Chen; Chihi-Yuan Lu

DiagBridge: Analyzing Scan Diagnosis Data in a Yield Perspective An
Yan Pan; Kannan Sekar; Atul Chittora; Shobhit Malik; Seng Keat Lim

The Importance of Reporting both Composite and Maze Yield for Process Split Yield Learning An
Fan Zheng; Amanda Piper; Gauri Karve; Kan Zhang; Yongchun Xin; Jang H Sim; Jason J Mazzotti

Session 2: Advanced Metrology 1
Silicon-Germanium (SiGe) Composition and Thickness Determination via Simultaneous Small-spot XPS and XRF measurements
Benoit Lherro; Wei Ti Lee; Mark Klare; Heath Pois; Mike Kwan; Saiqa Farhat; Jennifer Fullam; John Gaudiello; Srinivasan Rangarajan; Bing Sun; Nicolas Loubet; Qing Liu; Romain Wacquez; Sylvain Maitrejean; Tom Larson; Ying Wang; Emmanuel Augendre

Benefit of Combining Metrology Techniques for Thin SiGe Layers An
Delphine Le Cunff; Thomas Nguyen; R Duru; F. Abbate; Nicolas Laurent; Jonny Hoglund; Matthew Wormington; F. Pernot

New Interferometric Measurement Technique For Small Diameter TSV An
Padraig Timoney; Yeong-Uk Ko; Daniel W. Fisher; Alok Vaid; Sarasvathi Thangaraju; Daniel Smith; Ke Xiao; Tim Johnson; Holly Edmundson; Wonwoo Kim; Ramakanth Alapati; Himani Kamineni; Dingyou Zhang; Nigel Smith; Brennan Peterson; Hemant Amin; Jonathan Peak

Ellipsometry for cSiGe Metrology A n
Saiqa Farhat; Srinivasan Rangarajan; Timothy J. Mcardle; Michael Steigerwalt; Dawei Hu; Ming Dai

MBIR Characterization of Photosensitive Polyimide in High Volume Manufacturing An
Taher Kagalwala; Jonny Hoglund; Brian Erwin; Victoria Calero-DdelC; Yuri Brovman

Session 3: 3D/TSV
Successful Void Free Gap Fill of 3μm, High AR Via Middle, Through Silicon Vias at Wafer Level An

Sarasvathi Thangaraju; Luke England; Mohamed Rabie; Ding You Zhang; Kumarapuram Gopalakrishnan; Richard McGowan; Adam Selsley; Rudraskandan Giridharan; Si Peng Gu; Vijayalakshmi Seshachalam; Chen Wang; Shinichiro Kikita; Sudhir Baral; H. Edmundson

**Wafer Thinning for High-Density 3D-LSIs _12-Inch Wafer Level 3D-Integration at GINTI**
Mariappan Murugesan; Takafumi Fukushima; JiChel Bea; Hiroyuki Hashimoto; Yutaka Sato; Kang Wook Lee; Mitsumasa Koyanagi

**Use of Optical Metrology Techniques for Uniformity Control of 3D stacked IC’s**
Delphine Le Cunff; Manon Tardif; Jean-Philippe Piel; Gilles Fresquet; Nicolas Hotellier; Kyoto Le Chao; Lauren-luc Chapelon; Pierre Bar; Stephanie Eynard

**Analysis of TSV Geometric Parameter Impact on Switching Noise in 3D Power Distribution Network**
Huanyu He; Xiaoxiong Gu; James J.-Q. Lu

**RF Characterization of Through Silicon Vias Test Structures in a 3-Tier Stacked Wafer**
Min Xu; Robert Carroll; Harika Manem; Robert Geer

**3D Technology Applications Market Trends & Key Challenges**
Amandine Pizzagalli; Thibault Buisson; Rozalia Beica

**Session 4A: Advanced Process Control (APC)**
First Time Right Deposition of embedded SiGe in new Products
Raymond Van Roijen; Meghan Linskey; Eric Harley; Alyssa Herbert; Mohammed Fayaz; Michael Brodfuehrer; Anda Mocuta; Michael Steigerwalt; Colleen Snavely

Chamber Matching Across Multiple Dimensions: Utilizing Predictive Maintenance, Equipment Health Monitoring, Virtual Metrology and Run-To-Run Control
James Moyne; Manjunath Yedatore; Jimmy Iskandar; Parris Hawkins; John Scoville

FDC Run-to-Run Variation Monitoring for Sensor Level Diagnosis in Tool Condition Hierarchy
Jakey Blue; Jacques Pinaton; Agnès Roussy

**Session 4B: Factory Optimization**
300mm+ Factory Layout Design and Innovations for Advanced Semiconductor Manufacturing
Ming-Te Kao; Chia-Yin Kuo; Yih-Jan Huang; Fiona Lee; Rich Huang

Emerging Challenges to Carrier Logistics
Jan Rothe; Terry Asakawa; Gabriel Gaxiola; Makoto Yamamoto; Kenji Yamagata; Les Marshall

iPM – A Fab Preventive Maintenance Forecasting & Downtime Management Tool
Guy Senerman

**Session 5: Poster Session**
3D ICs in the Real World
Dick James
Advanced FOUP Purge Using Diffusers for FOUP Door-Off Application
Huaping Wang; Seong Chan Kim; Bo Liu

Advancement of Microelectronics-Grade Carbon Nanotube Materials for NRAM Device Manufacture
James E. Lamb III; Stephen Gibbons; Yongqing Jiang; Kay Mangelson; Kathryn Kremer; Dan Janzen; John Bledsoe; Mathew Boeser

Challenges and Opportunities in Atomistic Dopant Profiling Using Capacitance-Voltage Measurements
Samira Aghaei; Mohit Mehta; Petru Andrei; Mark J. Hagmann

Correlation Study of Spatial ESC Temperature Profile and Optical CD/CD SEM measurements to investigate silicon recess and gate CD after Etch
John Newby; Giampietro Bieli; Marcus Wollenweber; Robert Melzer; Thomas Nogatz; Jörg Sobe

Defect Engineering for Carrier Lifetime Control in High Voltage GaAs Power Diodes
Dr. Vladimir A. Kozlov; Dr. Fedor Y. Soldatenkov; Dr. Iren L. Shulpina; Dr. Valeri G. Danilchenko; Dr. Vladimir I. Korolkov

Development of Smart Feature Selection for Advanced Virtual Metrology
Benjamin Lenz; Bernd Barak; Carolin Leicht

Effective Testing for Wafer Reject Minimization by Terahertz Analysis and Sub-Surface Imaging
Anis Rahman; Aunik K. Rahman

Evaluation of FKM / PTFE Hybrid Material Seal
Ippei Nakagawa

Fluorine interaction on SICN and SIOC layers detected by fault detection
Jean-René Raguet; Laurent Blaya; Emmanuel Paire

Hidden Equipment Productivity Opportunities
Jochen Kinauer; Bert Müller

Highly-stable Four-point-probe Metrology in Implant and Epitaxy Processes
Qing Ye; Jianli Cui; Lu Yu; Tetyana Shapoval; Florian Flach; Ronny Haupt; Franz Heider; Walter Petersmann; Martin Haberjahn

Improvement of Characteristic of Redistribution Layer (RDL) on Mobile Application
C.S. Liu; Yu-Nu Hsu; Chyi-Tsong Ni; Ponder Pang; Justin Lo; Wallance Su; Chin-Yu Ku

Improving Yield through Elimination of Nitride Stringers in 180nm EEPROM Process Technology
Santosh Menon; Moshe Agam; Roger Young; Peter Cosmin; Sorin Georgescu

Mueller Matrix Optical Scatterometry of Si Fins Patterned using Directed Self-Assembly Block Copolymer Line Arrays
Dhairya J. Dixit; Alain Diebold; Brennan Peterson; Joe Race; Manasa Medikonda

**Multivariate Method for the Monitoring of Etch Chamber Insitu Cleaning**
Mohamed Boumerzoug; Suradej Promreuk

**Novel Metrology and Wafer Grinder Technologies Combine for Improved Capability for TSV Structures**
Russ Dudley; David Grant; Thomas Brake; David Marx; Rajiv Roy; Michael Kirkpatrick; Bill Kalenian

**Optical Technologies for TSV Inspection**
Arun Ananth Aiyer; Nikolai Maltsev; Jaeseok Ryu

**People Productivity Improvement via Cloud Machine Monitor**
Chun-Jung Huang; Yh Chen; CL Wang

**Rethinking the Approach to Higher 450mm Process Gas Flows: A Case Study**
William Corbin; Adrienne Pierce; Chris Bailey

**Scanning frequency comb microscopy (SFCM): A New Method Showing Promise for High-resolution Carrier Profiling in Semiconductors**
Mark J. Hagmann; Petru Andrei; Shashank Pandey; Ajay Nahata

**Screen Printed Flexible Pressure Sensors & Skin**
Saleem Khan; Leandro Lorenzelli; Ravinder Singh Dahiya

**Screening Scenario-based Analysis of Modifications in Planning of Semiconductor Manufacturing**
Marwa Attiya; Irfan A. Saadat; Ali Diabat

**Six Sigma in a Semiconductor Company**
Karen Riding; Dirk-Alexander Bruedern

**Surface Metal Contamination on Tool Components – A Case Study for Evaluating Acid Extraction ICP-MS Measurement Process**
Shi Liu; Bin Liu

**Uniformity Control for High Selective Down-Flow Plasma Etching on Silicon Oxide**
Chiu Yuan-Chieh; Fang-Hao Hsu; Lo Kuo-Feng; Lin Xin-Guan; Lee Hong-Ji; Lian Nan-Tzu; Yang Tahone; Chen Kuang-Chao; Lu Chih-Yuan; Chih Yuan Lu; Kuang Chao Chen; Han-Hui Hsu

**Using in-line Film Measurement as a Proxy for Device Matching to Speed up Process Change Qualification**
Chienfan Yu; Raymond Van Roijen; Shailesh Shah; Eric Woodard; Javier Ayala; Edward Sziklas
Tuesday, May 20, 2014

Session 6: Advanced Metrology II
CD-SEM Metrology Evaluation of Gate-All-Around Si Nanowire MOSFET with Improved Control of Nanowire Suspension by Using a Buried Boron Nitride Etch-Stop Layer
Shimon Levi; Ofer Adan; Maayan Bar Zvi; Amiad Conley; Ori Shoval; Guy Cohen; Leathen Shi; Sarunya Bangsaruntip; Alfred Grill; Deborah Neumayer

Air Gap CV Measurement for Doping Concentration in Epitaxial Silicon
Franz Heider; Johannes Baumgartl; Thomas Jaehrling; Peter Horvath

Addressing thin film thickness metrology challenges of 14nm BEOL layers
Zhiming Jhang; Ronny Haupt; Carlos Ygartua; Alok Vaid; Michael Lenahan; Vijayalakshmi Seshachalam

Assessment of minority-alloy component segregation (e.g. Mn, Al) in back end of line copper trench structures using Kelvin probe technique
Joyeeta Nag; Shishir Ray; Felipe Tijiwa-Birk; Kriteshwar K Kohli; Andrew H Simon; Siddarth A Krishnan; Christopher Parks

450mm Metrology and Inspection: The Current State and the Road Ahead
Rand Cottle; Nithin Yathapu; Katherine Sieg

Session 7: Defect Inspection I
Correlation Study of White Light Interferometer Measurements with Atomic Force Microscope Measurements for Post-CMP Dishing Measurements Applied to TSV Processing
Daniel W. Fisher; Padraig Timoney; Yeong-Uk Ko; Alok Vaid; Sarasvathi Thangaraju; Daniel Smith; Sung Pyo Jung; Ramakanth Alapati; Wonwoo Kim; Hemant Amin; Jonathan Peak; Tim Johnson

Detection Sensitivity Improvement on STI Module in 28nm process foundry logic node
Dan Koronel; Govinda Soni; Vijeet Gupta; Mirko Beyer; Tobias Gunther; Remo Kirsch; Torsten Billasch; Christophe Soonekindt; Robert Van Oostrum

Investigation of Novel Inspection Capability for 3D NAND Device Wordline Inspection
Andrew James Cross; Soon Kyu Lee; Seong-Min Ma; IlSeok Seo; Hyeon Sang Shih; Hyeon Soo Kim; Oksen Baris; DoOh Kim; Seung Hwan Lee; Steve Lange

Progress on background signal analysis of bare wafer inspection systems based on light scattering for III/V epitaxial layer growth monitoring
Sandip Halder; Yves Mols; Dieter vanden Heuvel; Gerhard Bast; Gavin Simpson; Milko Peikert; Marco Polli; Seong Ho You; Jan van Puymbroeck; Matty Caymax; Eric Vancoille; Nancy Nieuwborg; Neli Ulea

Early Detection of Pattern Defect on ADI Wafers
Robert Teagle; Erin Lavigne; Frank Wilhelm Mont; Fei Wang; HungYu Tien; YuanChi Chiang; Derek Tomlinson
Session 8: Equipment Reliability and Productivity Enhancement
Implementation of an Advanced Recipe Management System in a Fully Automated 300mm Fab
Andrew Lu; Jeff Hanan; Kevin Drinkwine; Gaurav Gupta; Andreas Weber; Dan Cogut; Matthias Hanisch; Gary Green; Robert Sinn

Study of Central Supply Methodology for Silica-Based CMP Slurry
JP Yu; C.N. Chang; SS Lien; HC Hsiao; KT Tsai

Extending Dry Pump Reliability on High-k ALD Furnaces
Kastumi Nishimura; Maiku Boger; Kazuki Ito

Laser Marking Equipment Process $0 Cost Productivity Improvement
Darin Moreira Anthony Vincent; Bhuvenesh Rajamony

Session 9: Contamination Free Manufacturing (CFM)
450mm Carrier Interoperability Effects on Particle Generation
Angelo Alaestante; Christopher Borst

A study on the Defect induced by Ambient Moisture and Ammonia During Perhydropolysilazane Spin on Glass Process
Jeongin Yoon; Jinho KIM; Juhyun PARK; Joonho Jang; Kwangshin LIM; Jongsu KIM

Surface treatment against bromine defectivity in plasma etch reactor
Yoann Goasduff; Patrice Laurens; Giuseppe Distefano; Marylaine Nguyen

Optimized BARC Films and Etch Byproduct Removal For Wafer Edge Defectivity Reduction
Mohamed Boumerzoug

Session 10: Data and Yield Management
Integrated System for Consumable Yield Analysis
Zhuqing Zong; Ute Nehring

Methodologies for fast Yield Ramp with Limited Engineering Resources by Utilizing Inline Defect data overlay to SRAM Bitmap failure and Logic Diagnostics
Venkatesan Muthumalai; Yoong Ern Ling; Ryan Lockwood; Ryan Ross; Michael WU; Steve White

Line Centering Yield Optimization Method
Jeanne Paulette Bickford; Erik L. Hedberg; Troy J. Perry; Kevin K. Dezfulian

Advanced Soft Fail Characterization Methodology for Sub-28nm Nanoscale SRAM Yield Improvement
Jianhua Yin; Sherwin Fernandes; Yinzhe Ma; Sheng Xie; Xuemei Liu; Qiushi Wang; Mark Dexter; Meixiong Zhao; Randy Mann; Chong Khiam Oh; Mark Tay; Seng Keat Lim; Dapeng Sun; Paulo Chao; Jeffrey Lam

Session 11: Discrete Power Devices/Emerging Technologies
New Modular High Voltage LDMOS Technology Based on Deep Trench Isolation and 0.18um CMOS Platform

Thursday, May 22, 2014

Session 11: Advanced Test and Measurement

Novel Non‐Invasive Test Methodologies for Embedded Memory Testing
John Fang;Mingchao Sun

Corrective Action for Recurrent Device Failures
M Christina S. Tsai;Sikhander Sohail;Rajeev Agarwal

Test and Measurement of High‐K Gate Dielectric Films
M. S. Hossain;S. Jayaraman;C. P. H. Tan;H. S. F. Yee;W. S. Koh;C. W. Tan;T. W. Gan;C. H. Chua;J. W. L. Ng

Process Optimization Strategies for Partial Reuse of Automotive Electronic Packaging
Thomas H. L. Yip;B. C. M. Ong;H. T. Ong;K. F. Y. Tan;W. T. S. Lu;W. S. S. Tan;M. N. C. Lee;C. V. G. Toh

Session 12: Advanced Design and Solution Verification

Power Management and Test Challenges for a High Performance Mobile Processor
Chandan Bhargava;Jing Tang;Jianjun Liu;Jingfeng Wu;Jingying Jiang;Zhenhua Zhang;Bing Guo;Mo Tu

Ultra‐Low Power Design for Advanced Battery‐Operated Applications
Shannan Cheng;Wei Wei;Zhaohui Lin;Rui Chen;Jian Li;Steffen Ritter;Kwok Fai Chan;Kwok Ng;Zhiwei Zhang;Zhiwen Zhai;Enrique Valera;Yang Yang;Sandip Sengupta;Luffy Di;Ming Cai

Dedicated low power microcontroller for High Dynamic Reactive Power control in Home Power Systems
Arman Naseri;Ali Kafash;Ali Safaei;Amirreza Farhadi

Session 13: Advanced Equipment and Materials II

The Effect of Backside Roughness on Al Interconnect Dimensions for RF CMOS SOI Devices
Shawn Adderly;Jeffrey Gambino;Matthew Moon;Jeffrey Hanrahan;Brett Cucci

Uniformity Improvement for 200 mm APCVD Epitaxial Si Films Enabled by Retrofit of Applied Materials Epi Centura
Matthias Künle;Johannes Baumgartl;Thomas Ackermann

A Systematic Methodology For Etch Chamber Matching To Meet Leading Edge Requirements
Stephen Hwang;Eric Tonnis

Process Monitoring Using Advanced Inspection Methodologies &ndash; a Study With CVD
Sandeep Gaan; Chandar Palamadai; ZhiGuo Sun; Sipeng Gu; Yang Bum Lee; Joey Li; Lingyan Zhao; Lucy Fan

Use of Diodes to Enable uLoop\textsuperscript{reg} Test Structures for Buried Defects and Voltage to $\kappa\psi$ Intensity Calibration
Oliver D. Patterson

Session 15: Advanced Equipment and Materials II
Comparison study between optical emission spectroscopy and x-ray photoelectron spectroscopy $\kappa\chi$ techniques during process etch plasma
Maria Rizquez; Anthony JAMES; Agnes Roussy; Jacques Pinaton; Yoann Goasduff

Etch Planarization - A New Way Of Correcting Post CMP Non-Uniformity $\kappa\psi$
Meihua Shen; Baosuo Zhou; Yifeng Zhou; John Hoang; Andrew Bailey; Eric Pape; Harmeet Singh; JIm Bowers; Rich Wise; Ravi Dasaka

A CMP Solution For Enabling STT-RAM Fabrication Using VIA-Less Process Flow $\kappa\psi$
Sajjad A. Hassan; Motoya Okazaki; Mahendra Pakala; Garrent Sinn

High-k/Metal Gates in the 2010s $\kappa\psi$
Dick James