Tuesday Oct. 28

Registration
Location: in front of Studio
08:30 – 09:00

SESSION: Opening
Location: Studio
09:00  WELCOME TO SOC 2014
Jari Nurmi, Tampere University of Technology, Finland

SESSION: Keynote 1
Location: Studio
Chair: Jari Nurmi, TUT, Finland
09:15  Challenges for Electronics Design in the Nano-Scale
Ricardo Reis, Universidade Federal do Rio Grande do Sul, Brazil

SESSION: Special Applications
Location: Studio
Chair: Geza Kolumban, Pázmány Péter Catholic University, Hungary
10:00  System on Chip Design of a Linear System Solver ..... 1
Bucek, Jiri; Kualik, Pavel; Lorenz, Robert; Zahradnicky, Tomas
Czech Technical University in Prague, Czech Republic
10:20  Adaptive Runtime Management of Heterogeneous MPSoCs: Analysis,
Acceleration and Silicon Prototype (PhD forum submission) ..... 7
Arnold, Oliver; Fettweis, Gerhard; TU Dresden, Germany

SESSION: Coffee break
Location: Rondo
10:40 – 11:25 Coffee and NORCHIP posters

SESSION: Design Analysis
Location: Studio
Chair: Claudio Brunelli, Microsoft, Finland
11:25  A Cycle-Accurate Network-on-Chip Simulator with Support for Abstract Task
Graph ..... 11
Joseph, Jan Moritz; Pionteck, Thilo; Universität zu Lübeck, Germany
11:45  Fast Memory Region: 3D DRAM memory concept evaluated for JPEG2000
algorithm ..... 17
Schoenberger, Alex; Hofmann, Klaus; TU Darmstadt, Germany
12:05  A Transaction-Level Framework for Design-Space Exploration of Hardware-
Enhanced Operating Systems ..... 21
Gregorek, Daniel; García-Ortíz, Alberto; University of Bremen, Germany

SESSION: Lunch
Location: Restaurant Fuuga
12:25 – 13:30
SESSION: Keynote 2  
Location: Studio  
Chair: Roberto Airoldi, NSN, Finland  
13:30 New approach for design and implementation of future communications systems  
Geza Kolumban, Pázmány Péter Catholic University, Hungary

SESSION: NORCHIP & SoC 2015 Announcement  
Location: Studio  
14:15 – 14:30

SESSION: Data-Path Optimizations  
Location: Studio  
Chair: Erno Salminen, TUT, Finland  
14:30 Optimal Data Path Widths for Energy- and Area-efficient Max-Log-MAP Based LTE Turbo Decoders  
Broich, Martin; Noll, Tobias G.; RWTH Aachen University, Germany  
14:50 Energy-efficiency of floating-point and fixed-point SIMD cores for MIMO processing systems  
Günther, Daniel; Bytyn, Andreas; Leupers, Rainer; Ascheid, Gerd  
RWTH Aachen University, Germany  
15:10 L2 ISA++: Instruction Set Architecture Extensions for 4G and LTE-Advanced MPSoCs  
Arnold, Oliver; Neumärker, Felix; Fettweis, Gerhard; TU Dresden, Germany

SESSION: Coffee break  
Location: Rondo  
15:30 - 16:00

SESSION: Physical Level Design Issues  
Location: Studio  
Chair: Peeter Ellervee, Tallinn University of Technology, Estonia  
16:00 Limits of gate-level power estimation considering real delay effects and glitches  
Meixner, Michael; Noll, Tobias G.; RWTH Aachen University, Germany  
16:20 Unbalanced Buffer Tree Synthesis to Suppress Ground Bounce for Fine-grain Power Gating  
Usami, Kimiyoshi 1; Miyauchi, Makoto 1; Kudo, Masaru 1; Takagi, Kazumitsu 1; Amano, Hideharu 2; Namiki, Mitaro 3; Kondo, Masaaki 4; Nakamura, Hiroshi 4  
1) Shibaura Institute of Technology, Japan; 2) Keio University, Japan; 3) Tokyo University of Agriculture and Technology, Japan; 4) The University of Tokyo, Japan  
16:40 Keyed Logic BIST for Trojan Detection in SoC  
Dubrova, Elena 1; Näslund, Mats 2; Carlsson, Gunnar 2; Smeets, Ben 2  
1) KTH, Sweden 2) Ericsson AB, Sweden

17:00 End of session
17:30 Bus transport

SESSION: Ice-Hockey  
Location: Hakametsä Ice Hall  
18:30 – 20:45

Bus transport after the game

SESSION: Supper  
Location: Brewery Restaurant Plevna, Itäinenkatu 8  
21:00 – 23:00
WEDNESDAY Oct. 29

SESSION: Invited 3
Location: Studio
Chair: Waqar Hussain, TUT, Finland
09:00 Untapped Opportunities for Manycore Communication Optimization
Hank Hoffmann, University of Chicago, IL, USA

SESSION: Alternative Computing Concepts
Location: Studio
Chair: Jari Nurmi, TUT, Finland
09:45 Soft-Core eFPGA for Smart Power Applications ..... 66
Cuppini, Matteo 1; Mucci, Claudio 2; Franchi Scarselli, Eleonora 1; Canegallo, Roberto 2
1) University of Bologna, Italy; 2) STMicroelectronics, Agrate Brianza, Italy
10:05 An Implementation of Auto-Memoization Mechanism on ARM-based Superscalar Processor ..... 70
Shibata, Yuuki 1; Tsumura, Takanori 1; Tsumura, Tomoki 1; Nakashima, Yasuhiko 2
1) Nagoya Institute of Technology, Japan
2) Nara Institute of Science and Technology, Japan

SESSION: Coffee break
Location: Rondo
10:25 - 11:00

SESSION: Design Methodology
Location: Studio
Chair: Tapani Ahonen, TUT, Finland
11:00 WOKE: A novel workflow model editor ..... 78
Salminen, Erno; Honkonen, Mikko; Matilainen, Lauri; Hämäläinen, Timo D.
Tampere University of Technology, Finland
11:20 Early Power-aware Design Space Exploration for Embedded Systems: MPEG-2 Case Study ..... 86
Ben Abdallah, Feriel 1; Trabelsi, Chiraz 2; Ben Atitallah, Rabie 2; Abed, Mourad 2
1) Institut Mines-Telecom, Telecom ParisTech, France
2) University of Valenciennes, France
11:40 Gamification of System-on-Chip Design ..... 94
Hämäläinen, Timo D.; Salminen, Erno; Tampere University of Technology, Finland
12:00 Formal Verification of Circuit-Switched Network on Chip (NoC) Architectures using SPIN ..... 102
Zaman, Anam; Hasan, Osman; National University of Science and Technology, Pakistan

SESSION: Lunch
Location: Restaurant Fuuga
12:20 – 13:30

SESSION: Invited 4
Location: Studio
Chair: Waqar Hussain, TUT, Finland
13:30 A Dynamically Reconfigurable Multi-ASIP Architecture for Multi-Standard and Multi-Mode Turbo Decoding
Vianney Lapôtre, Université de Bretagne-Sud, France
SPECIAL SESSION: Multicore and Manycore Architectures, Applications and Platforms
Location: Studio
Chair: Waqar Hussain, TUT, Finland

14:00  A Many-Core Hardware Acceleration Platform for Short Read Mapping Problems Using Distributed Memory Interface with 3D-stacked Architecture ..... 110
Liu, Pei; KTH, Sweden

14:20  Implementation of Multicore Communications API ..... 118
Virtanen, Janne; Matilainen, Lauri; Salminen, Erno; Hämäläinen, Timo D.; TUT, Finland

14:40  I/O Virtualization Utilizing an Efficient Hardware System-level Memory ..... 124
Kornaros, George; Harteros, Kostantinos; Christoforakis, Ioannis; Astrinaki, Maria
Technological Educational Institute of Crete, Greece

15:00  A Communication Model and Partitioning Algorithm for Streaming Applications for an Embedded MPSoC ..... 128
Kelly, Wayne 1; Fläskamp, Martin 2; Sievers, Gregor 2; Ax, Johannes 2; Chen, Jianing 1; Klarhorst, Christian 2; Ragg, Christoph 2; Jungeblut, Thorsten 2; Sorensen, Andrew 1
1) Queensland University of Technology, Brisbane, Australia
2) Bielefeld University, Germany

SESSION: Coffee break
Location: Rondo
15:20– 15:40

SPECIAL SESSION: Advances in High Performance Reconfigurable Architectures
Location: Studio
Chair: Tapani Ahonen, TUT, Finland

15:40  Constraint-Driven Frequency Scaling in a Coarse Grain Reconfigurable Array ..... 134
Hussain, Waqar 1; Hoffmann, Henry 2; Ahonen, Tapani 1; Nurmi, Jari 1
1) TUT, Finland; 2) University of Chicago, IL, USA

16:00  A Reconfigurable MapReduce Accelerator for multi-core all-programmable SoCs ..... 140
Kachris, Christoforos; Sirakoulis, Georgios; Soudris, Dimitrios
Democritus University of Thrace, Greece

16:20  Parallel and Distributed Simulation of networked Multi-Core Systems ..... 146
Wehner, Philipp; Göhringer, Diana; Ruhr-University Bochum, Germany

SESSION: Closing
Location: Studio
16:40 – 16:50

SESSION: Farewell Banquet
Location: Ristorante Como, Hämeenkatu 7
19:00 – 22:00