2014 IEEE 16th Electronics Packaging Technology Conference

(EPTC 2014)

Singapore
3-5 December 2014
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<td>John Hunt</td>
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- **W2W Permanent Stacking for 3D System Integration**
  Lan Peng, Soon-Wook Kim, Michael Soules, Markus Gabriel, Margarete Zoberbier, Erik Sleeckx, Herbert Struyf, Andy Miller and Eric Beyne

- **Stochastic Wire-length Model with TSV Placement on Periphery Area**
  Jianhui Ling, Huiyun Li, Guoqing Xu and Liying Xiong

- **Innovative Wafer Level Package Manufacturing with FlexLine TM**
  Seung Wook Yoon, Chen Kang, Kok Hwa Lim, Kenneth Seah and Yaojian Lin

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<td>Bill Chen</td>
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- **Extremely High Temperature and High Pressure (x-HTHP) Endurable SOI Device & Sensor Packaging for Deep Sea, Oil and Gas Applications**
  Daniel Rhee Min Woo, Jason Au Keng Yun, Yu Jun, Eva Wai Leong Ching and F. X. Che
Silver Screen Printed Transmission Lines- Analyzing the Influence of Substrate Roughness on the RF Performance up to 30 GHz
Ying Ying Lim, Yee Mey Goh, Manabu Yoshida, Tung Thanh Bui, Tracey Vincent, Masahiro Aoyagi and Changqing Liu

Characterization of Copper Conductive Ink for Low Temperature Sintering Processing on Flexible Polymer Substrate
Jaewon Kim, Byunghoon Lee, Jun Yan Lek, Riko I Made, Budiman Salam and Chee Lip Gan

High Power SiC Inverter Module Packaging Solutions for Junction Temperature over 220°C
Daniel Rhee Min Woo, Hwang How Yuan, Jerry Aw Jie Li, Ho Siow Ling, Lee Jong Bum, Zhang Songbai

Workability and Reliability Assessment of Various High Bandwidth PoP Structures
Mike Hung, Louie Huang, Timmy Lin, Eting Chen, Edward Huang and YC Ding

Etch-hole Design in Encapsulation for Better Robustness
Jae-Wung Lee, Jaibir Sharma, Srinivas Merugu and Navab Singh
BGA Packaging Using Insulated Wire for Die Area Reduction
Shailesh Kumar, Vikas Garg, Chetan Verma, Rishi Bhooshan, Poh Zi-Song and LC Tan

Design and Implementation of Two Different RF SiPs for Micro Base Station
Yi He, Fengman Liu, Peng Wu, Fengze Hou, Jun Li, Jie Pan, Dongkai Shangguan, Liqiang Cao

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A Fast Passive-Heating Setup to Investigate Die-Attach Delamination in Packaged Devices
Tiphaine Pélisset, Mirko Bernardoni, Michael Nelhiebel and Thomas Antretter

Effect of Additive Elements on Crack Propagation Behavior for Sn-Bi Solders at High Temperatures
Noritake Hiyoshi, Mitsuo Yamashita and Hiroaki Hokazono

Reliability Physics and Probabilistic Design for Reliability (PDfR): Role, Attributes, Challenges
E. Suhir
Interfacial Microstructure and Shear Strength of Sn-Ag-Cu Based Composite Solders on Cu and Au/Ni Metallized Cu Substrates
Tama Fouzder, Y. C. Chan and Daniel K. Chan

Challenges and Solutions on Pre-Assembly Processes for Thinned 3D Wafers with Micro-bumps on the Backside

Low Stress Die Attach Material Challenges for Critical Si Node with Cu Wire
Megan Chang and Anderson Li

The Study of Adhesive Performance Within Backside-Via Revealing
H. Y. Li, L. Ding and G. Q. Lo
**Session**: B1: Interconnection Technologies 1  
**Date/Time**: Thursday, 4th December 2014 / 14:00 – 15:20hrs  
**Venue**: Orchard Main Ballroom 4301AB  
**Chair(s)**: Hong Meng Ho

- **Advanced Electrical Array Interconnections for Ultrasound Probes Integrated in Surgical Needles**  
  Giuseppe Schiavone, Thomas Jones, Dennis Price, Rachael McPhillips, Zhen Qiu, Christine E. M. Demore, Yun Jiang, Carl Meggs, Syed O. Mahboob, Sam Eljamel, Tim W. Button, Sandy Cochran and Marc P. Y. Desmulliez

- **Sintering of Ag Paste for Power Devices Die Attach on Cu Surfaces**  
  Vemal Raja Manikam and Erik Nino Tolentino

- **Bondability and Challenges of Cu Ultra-Fine-Wire Bonding**  
  Sylvia Sutiono, Zhangxi, Tok Chee Wei, Don Syth An, Murali Sarangapani, Louie Huang, Jason Hung and Frank Lin

- **Breakthrough Development of Ultimate Ultra-Fine Pitch Process with Gold Wire & Copper Wire in QFN Packages**  
  C. E. Tan, J. Y. Liong, Jeramie Dimatira, Lee Wee Kok, Jason Tan, Lie Handra Wijaya, James Song, Teshima Satoshi and K. H. Kwong
### B2: Electrical Modelling 1

**Date/Time:** Thursday, 4th December 2014 / 14:00 – 15:20hrs  
**Venue:** Orchard Main Ballroom 4302  
**Chair(s):** Wui Weng Wong

- **A Low-Cost, High Efficiency Power Architecture Map for Basic and Performance Level Tablet Computers**  
  *Suvankar Biswas and Ripan Das*

- **Measurement of Power Distribution Network Impedance Using an Error Analysis Approach**  
  *Eng-Kee Chua, Xing-Ming Li, Shan-Qing Hu and Kye-Yak See*

- **Vertical Interconnections using Through Encapsulant Via (TEV) and Through Silicon Via (TSV) for High-Frequency System-in-Package Integration**  
  *M. Wojnowski, K. Pressel, G. Beer, A. Heinig, M. Dittrich and J. Wolf*

- **Capacitive Crosstalk Compensation Structure for Improved High-Speed On-Package Signaling**  
  *Bok Eng Cheah, Jackson Kong, Ping Ping Ooi, Kok Hou Teh and Po Yin Yaw*

### B3: Advanced Packaging 2

**Date/Time:** Thursday, 4th December 2014 / 14:00 – 15:20hrs  
**Venue:** Orchard Main Ballroom 4303  
**Chair(s):** John Oviso

- **Air-Gap in Encapsulation for Fast Release and Safe Sealing**  
  *Jae-Wung Lee, Srinivas Merugu, Jaibir Sharma, Geng Li and Navab Singh*
The Study of High-Lead Solder Joints Reliability of Flip Chip Devices
Lingjuan Tian, Yuanfu Zhao, Quanbin Yao, Yusheng Cao and Binhao Lian

Elongated Copper Pillar Bump Flip Chip Design on Molded Interconnect Substrate (MIS) for Advanced Flip Chip Packages
Ho Siow Ling, Sherryl Alialy, Stephenie, Zhang Xiaowu and Raymond Shoa Siong Lim

Structure Reliability and Characterization for FC Package w/ Embedded Trace Coreless Substrate
Eason Chen, Albert Lan, Jack You and Mark Liao

Session | B4: Quality & Reliability 2
Date/Time | Thursday, 4th December 2014 / 14:00 – 15:20hrs
Venue | Orchard Main Ballroom 4202
Chair(s) | Tong Yan Tee

Development of Scanning Acoustic Microscopy Method with Passive Integration Package for Mass Production Monitoring
C.T. Tai, C.Y. Lai and Subramanian Eswariy

Intermetallic Compound Growth Mechanism and Failure Modes of Flip Chip Solder Bump with Different UBM Structure during Electromigration
Yong-Sheng Zou, Yu-Hsiang Hsiao and Kwang-Lung Lin

Analysis of Silicone-Based Adhesive Bond Separation
L. E. Khoong, T. K. Gan and M. B. Young
Copper Ball Bond Shear Test for Two Pad Aluminum Thicknesses
Derek Andrews, Levi Hill, Aaron Collins, Kok Inn Hoo and Stevan Hunter

Session B5: Materials & Processes 2
Date/Time Thursday, 4th December 2014 / 14:00 – 15:20hrs
Venue Orchard Main Ballroom 4203
Chair(s) L. C. Tan

Flip Chip Die Attach Flux Evaluation Method
Adam Liu, Tank Lo, James Li, Eason Chen, JZ Yang and CT Chen

Simultaneously Obtaining the Young’s Relaxation Modulus and Shear Relaxation Modulus of an Epoxy Molding Compound by Using DMA
Dao-Long Chen, Tz-Cheng Chiu, Tei-Chen Chen, Ping-Feng Yang, Chih-Pin Hung and Jen-Kuang Fang

Picking Large Thinned Dies with High Topography on Both Sides
Carine Gerets, Jaber Derakhshandeh, Teng Wang, Giovanni Capuz, Arnita Podpod, Caroline Demeurisse, Kenneth June Rebibis, Andy Miller, Gerald Beyer and Eric Beyne
**Session** | C1: Quality & Reliability 3  
**Date/Time** | Thursday, 4th December 2014 / 15:50 – 16:50hrs  
**Venue** | Orchard Main Ballroom 4301AB  
**Chair(s)** | Che Faxing

- **An Alternative Methodology of Determining the Package Delamination Failure Starting Point Using the Thermomechanical Analyzer**  
  *Aaron D. Cadag and Bernie Chrisanto M. Ang*

- **Towards Adequate Qualification Testing of Electronic Products: Review and Extension**  
  *G. Khatibi, B. Czerny, J. Magnien, M. Lederer, E. Suhir and J. Nicolics*

**Session** | C2: Wafer Level Testing  
**Date/Time** | Thursday, 4th December 2014 / 15:50 – 16:50hrs  
**Venue** | Orchard Main Ballroom 4302  
**Chair(s)** | Bruce Kim

- **Thickness Dependency of Adhesion Properties of TiW Thin Films**  
  *A. Roshangias, R. Pelzer, G. Khatibi and J. Steinbrenner*

- **Concurrent System Level Test (CSLT) Methodology for Complex System-on-Chip**  
  *Dilip Kumar Reddy Tipparthi and Karthik Krishna Kumar*
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- **Flip Chip Packaging with Pre-Molded Coreless Substrate**
  *Tom Tang, Albert Lan, Jensen Tsai, Ivan Chang and Evan Chen*

- **Study on Electrical Characteristics for Active Die Embedding Substrate**
  *Hyunho Kim*

- **Temporary Handling Technology for Advanced Wafer Level Packaging Applications Based on Adhesive Bonding and Laser Assisted De-Bonding**
  *Kai Zoschke, Thorsten Fischer, Hermann Oppermann and Klaus-Dieter Lang*

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<td>Eric Yong</td>
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- **Manufacturability Readiness of Insulated Cu Wire Bonding Process in PBGA Package**
  *Leong HungYang, Yap BoonKar, Tan Chou Yong, Navas Khan, Mohd Rusli Ibrahim, L. C. Tan*
Wirebond Enhancement on Copper Palladium Bonding in a Over Pad Metalization

Michael B. Tabiera, Bryan Christian S. Bacquian and Terencio D. Lacuesta

Process Development and Optimization for High Temperature Endurable Flip Chip Interconnection in SiC High Power Module

Jie Li Aw, Bu Lin, Hwang How Yuan and Daniel Rhee Min Woo

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High Temperature Die Attach Material on ENEPIG Surface for High Temperature (250DegC/500hour) and Temperature Cycle (-65 to +150DegC) Applications

Leong Ching Wai, Seit Wen Wei, Hwang How Yuan and Daniel Rhee MinWoo

Functionalised Copper Nanoparticles as Catalysts for Electroless Plating

R. E. Litchfield, J. Graves, M. Sugden, D. A. Hutt and A. Cobley

Fabrication and Characterization of Gold-Tin Eutectic Bonding for Hermetic Packaging of MEMS Devices

Eyup Can Demir, M. Mert Torunbalci, Inci Donmez, Y. Eren Kalay and Tayfun Akin
Poster Session 1

- **New Process Flow to Make QFN Package with Stand-Off**
  Peng Liu, Ping Wu and Q. C. He

- **60GHz Wideband Yagi-Uda Antenna Integrated on 2.5D Through Silicon Interposer**
  Songbai Zhang, Ka Fai Chang, Cheng Jin, Guruprasad Katti, Roshan Weerasekera and Surya Bhattacharya

- **Embedded Compact BaTiO 3-Polymer Film VHF Band-Pass Filter**
  Wenhu Yang, Shuhui Yu, Rong Sun and Wei-Hsin Liao

- **A Compact and Low-profile GaN Power Amplifier Using Interposer-Based MMIC Technology**
  Dongsu Kim, Jong Min Yook, Sung Jin An, Sung Ryul Kim, Jong-Gwan Yook and Jun Chul Kim

- **Through Silicon via (TSV) Scallop Smoothening Technique**
  Goon Heng Wong, Guan Kian Lau, King Jien Chui and Woon Leng Loh

- **2.5D Through Silicon Interposer Package Fabrication by Chip-on-Wafer (CoW) Approach**
  S. W. Ho, Mian Zhi Ding, Pei Siang Lim, Daniel Ismail Cereno, Guruprasad Katti, Tai Chong Chai and Surya Bhattacharya

- **Fabrication of Dielectric Insulation Layers in TSV by Different Processes**
  Zhenzhong Yong, Hengfu Li and Wenqi Zhang
Novel Spray Coating Process with Polymer Material Applied in CIS Wafer-Level-Packaging
Yuechen Zhuang, Daquan Yu, Fengwei Dai, Zhongcai Niu, Wenqi Zhang and Guoping Zhang

Development of Fluxless Bonding Using Deposited Gold-Indium Multi-Layer Composite for Heterogeneous Silicon Micro-Cooler Stacking
B. L. Lau, Yong Han H. Y. Zhang, L. Zhang and X. W. Zhang

Performance of Electrically Conductive Adhesive Attached Sensors in High Temperature Cycling
Sanna Lahokallio and Laura Frisk

Study of Intermetallic Compound Growth and Failure Mechanisms in Long Term Reliability of Silver Bonding Wire
You Cheol Jang, So Yeon Park, Hyoung Dong Kim, Yeo Chan Ko, Kyo Wang Koo, Mi Ri Choi, Hyung Giun Kim, Nam Kwon Cho, Tae Kang, Jae Hak Yee, Sung Hwan Lim

Electrical Measurement and Analysis of TSV/RDL for 3D Integration
Xin Sun, Runiu Fang, Yunhui Zhu, Xiao Zhong, Yuan Bian, Shenglin Ma, Min Miao, Jing Chen, Yan Wang and Yufeng Jin

Integrated Electronic and Microfluidic Packaging for CMOS Biosensor Chip
Mian Zhi Ding, Chaitanya Kantak, Vempati Srinivasa Rao, Mi Kyoung Park and Chee Chung Wong
Biocompatible Packaging for Implantable Miniaturized Pressure Sensor Device used for Stent Grafts: Concept and Choice of Materials
Sabine Kirsten, Martin Schubert, Markus Braunschweig, Gregor Woldt, Tetiana Voitsekhivska, Klaus-Jürgen Wolter

Package Characterization of FET-Based Biochemical Sensors
Tetiana Voitsekhivska, Eike Suthau, Sabine Kirsten, Martin Schubert, Felix Zörgiebel, Gianaurelio Cuniberti and Klaus-Jürgen Wolter

Inkjet Printed Transmission Line Elements for RF Applications and Measurement Challenges
Nishshanka Bandara Narampanawe, See Kye Yak and Zhang Jie

One-Sided Directional Slot Antenna with Impedance Matching Circuit for 3D Packaging
Haruichi Kanaya, Naoto Iizasa and Tomoki Oda

Sequential Stress Combinations in Product Level Reliability Testing of Industrial Electronics
J. Pippola, T. Marttila and L. Frisk

How to Improve Void Performance in Wafer Bumping
Zhang Ruifen, Yap Kong Tat, Yam Lip Huei and Reynoso Dexter

Optimization of the Wafer Level Molding Process for High Power Device Module
Lin Bu, Siow Ling Ho, Sorono Dexter Velez and Daniel Rhee Min Woo
Single & Multi Beam Laser Grooving Process Parameter Development and Die Strength Characterization for 40nm Node Low-K/ULK Wafer
Koh Wen Shi, K. Y. Yow and Calvin Lo

Joint Strength and Microstructures of Brazed Joints of Stainless Steel with Fe-based Filler
Takahiro Tsunoda, Kangdao Shi, Ikuo Shohji, Kotaro Matsu and Yasuhiro Taguchi
### Session D1: Advanced Packaging 4

**Date/Time:** Friday, 5th December 2014 / 08:30 – 10:10hrs  
**Venue:** Orchard Main Ballroom 4301AB  
**Chair(s):** Bok Eng Cheah

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<td>Electrical Performance Characterization for Novel Multiple Compartments Shielding and Verification on LTE Modem SiP</td>
<td>Albert Lin, Vincent Chen, JJ Chen, Simon Leou, Thomas Wang and Harrison Chang</td>
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<td>Alternative Package-on-Package with Organic Substrate Interposer for Stacking Packaging Solution</td>
<td>Steven Lin, Mark Liao, Albert Lan and David Wang</td>
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<td>Photonic Device Package Design, Assembly and Encapsulation</td>
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<td>Ultrahigh Speed Transceiver Package with Stacked Silicon Integration Technology</td>
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Date/Time | Friday, 5th December 2014 / 08:30 – 10:10hrs
Venue | Orchard Main Ballroom 4302
Chair(s) | Weerasekera Roshan

- Integrated Passive Devices on Through Silicon Interposer with Redistribution Layers  
  *Cheng Jin, Guruprasad Katti and Songbai Zhang*

- Capacitor Selection Process for High-Speed Power Distribution Network Based on Switching Current Requirement  
  *Xing-Ming Li, Shan-Qing Hu, Kye-Yak See and Eng-Kee Chua*

- Segmented Plated-Thru-Hole Design in Flip-Chip Packaging for Improved Electrical Performance  
  *Jackson Kong, Bok Eng Cheah, Chin Lee Kuan and Ping Ping Ooi*

- Electromagnetic Modelling and Simulation of TSVs in 2.5D Interposers for RFICs  
  *Kaushal Kannan and David Crouse*

- Study of Transmission Line Performance on Through Silicon Interposer  
  *Ka Fai Chang, Rui Li, Liang Ding and Songbai Zhang*
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1. **Comprehensive Study on Reliability of Chip-Package Interaction Using Cu Pillar Joint onto Low k Chip**  
   *F. X. Che, Jong-Kai Lin, K. Y. Au and Xiaowu Zhang*

2. **Evaluating the Optimal Location for Embedded Accelerometers using Experimentally Validated Computer Algorithms**  
   *Guy Banwell, Richard Sharpe, Paul Conway and Andrew West*

3. **Wirebondability Enhancement for Very Small Die in Power Packages with Dynamic Simulation**  
   *Xueren Zhang, Kim-yong Goh, Yiyi Ma, Tito Verano, Raquel Fundan, Wingshenq Wong and Loic Renard*

4. **Unit Warpage Control with Universal Die Thickness**  
   *Gu Bin, Jun Dimaano Jr., Richen Chen, Eric Bool, Seow Fui Shi, Choon Ghee Ang and Nathapong Suthiwongsunthorn*

5. **Thermal Effects of TSV (Through Silicon via) with Void**  
   *Yunna Sun, Hui-Yeol Kim, Yan Wang, Guifu Ding, Junhong Zhao and Hong Wang*
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<td><strong>Process Development of Multi-Die Stacking Using 20 um Pitch Micro Bumps on Large Scale Dies</strong></td>
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<td>Lee Jong Bum, Jerry Aw Jie Li and Daniel Rhee Min Woo</td>
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<td><strong>Tunable 3D TSV-Based Inductor for Integrated Sensors</strong></td>
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<td><strong>Wafer to Wafer Bonding Using CuSn Microbumps for GaN-LED Substrate Transfer Process</strong></td>
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<td><strong>Package-Level Si-Based Micro-Jet Impingement Cooling Solution With Multiple Drainage Micro-Trenches</strong></td>
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<td>Yong Han, Boon Long Lau, Hengyun Zhang and Xiaowu Zhang</td>
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Experimental Characterization of Si Micropillar Based Evaporator for Advanced Vapor Chambers
Mengyao Wei, Sivanand Somasundaram, Bin He, Qian Liang, Chuan Seng Tan and Evelyn N. Wang

The Effect of Variation of Doping Density on Thermal Properties of Power Si MOSFET
Risako Kibushi, Tomoyuki Hatakeyama, Shinji Nakagawa and Masaru Ishizuka

Comparative Analysis of Novel Thermal Interface Containing Nano Additives
Przemysaw Matkowski, Tomasz Faat and Andrzej Mościcki

Design Considerations on the External Heat Exchanger for Cooling of Microelectronic Devices
H. Y. Zhang, X. W. Zhang, Y. Han, B. L. Lau, Hector Valladares, Hikmat Chammas and Bruce Bolliger

Session | E1: Quality & Reliability 4
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Date/Time | Friday, 5th December 2014 / 10:40 – 12:20hrs
Venue | Orchard Main Ballroom 4301AB
Chair(s) | John Pang

Experimental Study of Water Absorption of Electronic Components and Internal Local Temperature and Humidity into Electronic Enclosure
Hélène Conseil, Morten S. Jellesen and Rajan Ambat
Thermal and Mechanical Reliability of Low-Temperature Solder Alloys for Handheld Devices
Morgana Ribas, Sujatha Chegudi, Anil Kumar, Ranjit Pandher, Rahul Raut, Sutapa Mukherjee, Siuli Sarkar and Bawa Singh

Sensor-Enabled PCBs to Aid Right First Time Manufacture Through Defect Prediction
Richard Sharpe, Guy Banwell, Paul P. Conway and Andrew A. West

Growth Behavior and Physical Response of Al-Cu Intermetallic Compounds
Rainer Pelzer, Stefan Woehlert, Heinrich Koerner, Golta Khatibi and Juergen Walter

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Temporary Bonding on the Move Towards High Volume: A Status Update on Cost-Of-Ownership
Thomas Uhrmann, Jürgen Burggraf, Harald Wiesbauer, Julian Bravin, Thorsten Matthias, Markus Wimplinger and Paul Lindner

Influence of the Height of Carbon Nanotubes on Hot Switching of Au/Cr-Au/MWCNT Contact Pairs
H. Liu, A. P. Lewis, S.H. Pu, L. Jiang, J. W. McBride
Plasma Technology Optimization for a Robust Flip Chip Package

Thermo-Compression Bonding for 2.5D Fine Pitch Copper Pillar Bump Interconnections on TSV Interposer
Sharon Pei-Siang Lim, Mian Zhi Ding, Sorono Dexter Velez, Daniel Ismael Cereno, Jong Kai Lin and Vempati Srinivasa Rao

Wafer Level Underfill Study for High Density Ultra-fine Pitch Cu-Cu Bonding for 3D IC Stacking
Ling Xie, Sunil Wickramanayaka, Boo Yung Jung, Jerry Aw Jie Li, Lim Jung-Kai and Daniel Ismael

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Board Level Drop Test Simulation Using Explicit and Implicit Solvers
Yiyi Ma, Kim-Yong Goh and Xueren Zhang

Finite Strain Thermomechanical Material Characterization of Adhesives Used in Automotive Electronics for Quantitative Finite Element Simulations
B. Öztürk, P. Gromala, C. Silber, K. M. B. Jansen and L. J. Ernst
Chip Scale Package with Low Cost Substrate Evaluation and Characterization
Vito Lin, Vincent Lin, Nicholas Kao, Don Son Jiang and C. S. Hsiao


Effect of Thermo-Mechanical Excursions on Growth of Interfacial Intermetallic Compounds in Cu/Sn-Ag-Cu Solder Joints
Rituparna Ghosh, Praveen Kumar and Abha Misra

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Thermal Compression Bonding with Non-Conductive Adhesive of 30μm Pitch Cu Pillar Micro Bumps on Organic Substrate with Bare Cu Bondpads
Jie Li Aw, Alvin Chow, K. Y. Au and Jong-Kai Lin

Reliability of 3D Package Using Wafer Level Underfill and Low CTE Epoxy Mold Compound Materials
New Nano Size Filled TIM Material With High Thermally Conductive Properties
A. Mościcki, T. Faat, A. Kinart, A. Smolarek and E. Merten

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Sinter Paste for Power Packages
Yong Ling Xin

Application and High Temperature Storage Test on Zn-Al-Ge High Temperature Solder for Die Attach
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A 24 GHz Microstrip Grid Array Antenna Excited by Coaxial-Fed Slot
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- **Chip Package Interaction Induced ILD Integrity Issues in Fine Pitch Flip Chip Packages**  
  *Vikas Gupta, Shawn O’Connor and Charles Pilch*

- **Gold-Germanium Laser Jetting for High Temperature (300°C) Flip Chip Application**  
  *Hwang How Yuan, Ding Mian Zhi and Daniel Rhee Min Woo*

- **Advanced Thermocompression Flip Chip Bonding**  
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- **Package characterization of UTAC’s Grid Array Package (GQFN) and Performance Comparison over Standard Laminate Packages**  
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*Kejun Zeng and Amit Nangia*

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*Helen S. Villanueva, Manolo G. Mena and Prospero C. Naval*

The IMC Formation and Progress in the Copper Pillar Cu/Sn1.8Ag /OSP-Cu Microbump Structure upon Current Stressing  
*Chiao-Wen Chen, Kwang-Lung Lin, Ying-Ta Chiu, Chin-Li Kao, Chiu-Wen Lee and Ping-Feng Yang*

Leadfree Solder Joint Improvement Study  
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Basic Evaluation of Au Micro-Bumps Formed by Cyanide-Free Electroless Au Plating Process  
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Takanori Shuto, Keiichiro Iwanabe, Mutsuo Ogura, Katsuhiko Nishida and Tanemasa Asano

Magnetically Responsive SAC305 Solder for Precision Melting Applications
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Laminating Thin Glass Onto Glass Carrier to Eliminate Grinding and Bonding Process for Glass Interposer
Leon Tsai, Bor Kai Wang, Aric Shorey, Alvin Lee, Jay Su, Baron Huang, Wen-Wei Shen, Hsiang-Hung Chang and C. H. Chien

Influence of Mold Compound Type Towards Palladium Doped and Copper Doped 2N Au wire
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Advanced Interconnect Equipment and Process Development
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Power QFN Down Bond Lift and Delamination Study
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Thermo-Compression Bonding Assembly Process and Reliability Studies of Cu Pillar Bump on Cu/Low-K Chip
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Aging Effect on Creep Properties of SnBi Solders

Masao Sakane, Kota Yagi, Takamoto Itoh, Mitsuo Yamashita and Hiroaki Hokazono

Alternative Flip Chip Sample Preparation Technique Using Triple Ion Beam Milling

W. Qiu, B. Zee, F. J. Foo and W. Grünewald

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Enhanced Stitch Bonding Concept for QFN Package's Cu Wirebonding Process

Allen M. Descartin, Zhang XiaoLong, Sun Deguo, Li Jun and Yan BeiYue

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Analysis of Concurrent Failure Mechanisms in IGBT Structures During Active Power Cycling Tests

Zoltan Sarkany, Andras Vass-Varnai and Marta Rencz

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- **Comparison of Aluminum Post Etch Cleaning on MEMS Structures Using Formulated Organic Solvent Cleaners**
  *Lee Hou Jang Steven, Vladimir Bliznetsov, Deng Wei, Tham Dexian and Sunil Wickramanayaka*

- **Optimization Studies of Lift-Off Methods and its Application in Electrochemical Biosensors**
  *Leong Yew Wing, Zhang ShiYun, Christopher Pang, Mohammad Hazren, Sunil Arya Kumar and Wong Chee Chung*

- **Considerations for Package Routing for DRAM and NAND Flash Memory**
  *Wang Ai-Chie and Chong Chin Hui*

- **Effect of Temperature on Tensile Properties of High-melting Point Bi System Solder**
  *Haidong Zhang, Ikuo Shohji, Masayoshi Shimoda and Hirohiko Watanabe*

- **Mechanical Properties of Low-Silver Sn-1.0Ag-0.7Cu-1.6Bi-0.2In Solder**
  *Yuki Takahashi and Ikuo Shohji*

- **Tensile Properties of Low-melting Point Sn-Bi-Sb Solder**
  *Yuto Kubota, Ikuo Shohji, Tetsuyuki Tuchida and Kiyotomo Nakamura*

- **Effect Of Copper Roughness On Dielectric Adhesion**
  *Serine Soh Siew Boon, David Ho SW, Ding Liang and Sek Soon Ann*
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Improving Performance and Reliability of 3D Wafer Level Packaging with Unique Polymer Coating Process
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