2014 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference

(S3S 2014)

Millbrae, California, USA
6-9 October 2014
SESSION 1: Plenary Session

**8:20am**

Sequoia

**SESSION CHAIRS**

Olivier Faynot, CEA-Leti ● Steven Vitale, MIT Lincoln Laboratory ●
Zvi Or-Bach, MonolithIC 3D

8:20am 1.1  **The Role of the Cloud in Machine to Machine & Internet of Things Computing: Best Practices, Key Insights and Guidance to connecting devices to the cloud**
Bruno Terkaly; Microsoft, San Francisco, CA (invited talk)

9:00am 1.2  **10 Years of ULV: A Look Back and Where Do We Go From Here?**
Alice Wang; MediTek (invited talk)

9:40am 1.3  **Key Technology Trends and Their Impact on the Future of the Semiconductor Industry**
Mark Edelstone; Morgan Stanley Investment Banking (invited talk)

SESSION 2A: SOI Platforms

**10:40am**

Sequoia

**SESSION CHAIR**

Joao Antonio Martino, University of São Paulo

10:40am 2a.1  **Advanced High K/Metal SOI technologies for 32nm and Beyond**
M. Horstmann; Global Foundries, Dresden, Wilschdorfer, Landstraße (invited talk)

11:20am 2a.2  **28nm FDSOI: Platform and Products**
P. Flatresse; STMicroelectronics (invited talk)
SESSION 2B:
SubVt – Analog and RF
10:40am
Redwood

SESSION CHAIR
Jing Xie, Qualcomm Research

10:40am 2b.1 Boltzmann Energetics of Neuromorphic Systems N/A
G. Cauwenberghs; UC San Diego (invited talk)

11:20am 2b.2 A 361nA Thermal Run-away Immune VBB Generator Using Dynamic 7
Substrate Controlled Charge Pump for Ultra Low Sleep Current Logic on
65nm SOTB
H. Nagatomi1, N. Sugii2, S. Kamohara2, K. Ishibashi1; 1The University of Electro-
Communications, 2Low-power Electronics Association & Project

11:40am 2b.3 A 53μW -82dBm Sensitivity 920MHz OOK Receiver Design Using Bias 9
Switch Technique on 65nm SOTB CMOS Technology
H.M. Thien1, N. Sugii2, K. Ishibashi1; 1The University of Electro-
Communications, 2Low-power Electronics Association & Project

SESSION 3A:
FinFET
1:00pm
Sequoia

SESSION CHAIRS
Maud Vinet, CEA-Leti ● Ali Khakifirooz, Spansion

1:00pm 3a.1 SOI FinFET versus Bulk FinFET for 10nm and Below 11
T.B. Hook1, F. Allibert12, K. Balakrishnan14, B. Doris2, D. Guo2, N. Mavilla5, E. Nowak1, G. Tsutsui2,
R. Southwick2, J. Strane5, X. Sun2; 1IBM SRDC Essex Junction, VT, 2IBM Albany, NY, 3SOITEC
Albany, NY, 4IBM Yorktown Heights, NY, 5IBM Bangalore (invited)

1:40pm 3a.2 High Mobility Ω-Gate Nanowire P-FET on cSGOI Substrates Obtained by 14
Ge Enrichment Technique
P. Nguyen1, 3, S. Barraud1, M. Koyama1, M. Cassé1, F. Andrieu1, C. Tabone1, F. Glowacki1,
J.-M. Hartmann1, V. Maffini-Alvaro1, D. Rouchon1, N. Bernier1, D. Lafond1, M.-P. Samson2,
F. Allain1, C. Vizioz1, D. Delprat1, B.-Y. Nguyen3, C. Mazuré3, O. Faynot1, M. Vinet1;
1CEA-LETI, Minatec campus, Grenoble Cedex, France, 2STMicroelectronics Crolles, France, 3SOITEC, Bemin, France
2:00pm 3a.3 Dielectric Isolated FinFETs on Bulk Substrate 16
D. Lu1, K. Cheng1, P. Morin2, N. Loubet1, T. Hook1, D. Guo1, A. Khakifirooz1, P. Oldiges1,
B. Doris1, K. Rim1, A. Jacob3, H. Bu1, M. Khare1; 1IBM Research, Albany, NY,
2STMicroelectronics, 3GLOBALFOUNDRIES

2:20pm 3a.4 Elastic Relaxation in Intrinsically-Strained Fins: Simulations, Physical 18
and Electrical Characterization
F. Allibert1, P. Morin2, H. He3, J. Li3, W. Schwarzenbach1, N. Loubet2, A. Khakifirooz3, *,
B. DeSalvo4, B. Doris3; 1SOITEC, Bernin, France, 2STMicroelectronics, 3IBM Research, 4CEA-Leti
at Albany Nanotech, Albany, NY, *now with Spansion, Inc.

SESSION 3B:
SubVt – Digital
1:00pm
Redwood

SESSION CHAIR
Adrian Ionescu, École Polytechnique Fédérale de Lausanne

1:00pm 3b.1 Toward Robust Subthreshold Circuit Design: Variability and Soft Error 21
Perspective
M. Hashimoto; Dept. Information systems Engineering, Osaka University, Japan & JST, CREST
(invited talk)

1:20pm 3b.2 Energy Efficiency Benefits of Subthreshold-Optimized Transistors for Digital 23
Logic
P.J. Grossmann, S.A. Vitale, P.W. Wyatt; MIT Lincoln Laboratory, Lexington, MA

2:00pm 3b.3 Ultra-Wide Voltage Range 32-bit RISC CPU with Timing-Error 25
Prevention in 28nm CMOS
M. Hiienkari1, J. Teittinen1, L. Koskinen1, M. Turnquist2, M. Kaltiokallio2, J. Mäkipää3,
A. Rantala3, M. Sopanen3; 1University of Turku, Technology Research Center, Turku, Finland,
2Aalto University Department of Micro And Nanosciences, 3VTT Technical Research Centre
of Finland

2:20pm 3b.4 A Reduced-Memory FIR Filter Using Approximate Coefficients for 27
Ultra-Low Power SoCs
A.Klinefelter, B.H. Calhoun; University of Virginia, Charlottesville, VA
SESSION 4:
Special Invited 3D Hot Topics
1:00pm
Sequoia

SESSION CHAIR
Zvi Or-Bach, MonolithIC 3D

3:00pm  4.1  Monolithic 3D Integration: a powerful alternative to classical 2D scaling  29
M. Vinet¹, P. Batude¹, C. Fenouillet-Beranger¹, F. Clermidy¹, L. Brunet¹, O. Rozeau¹, J.M. Hartmann¹, O. Billoy¹, G. Cibrario¹, B. Previtali¹, C. Tabone¹, B. Sklenard¹, O. Turkyilmaz¹, F. Ponthenier¹, N. Rambal¹, M.P. Samson², F. Deprat¹, V. Lu², L. Pasini², S. Thuries¹, H. Sarhan¹, J.-E. Michallet¹, O. Faynot¹; ¹CEA-Leti, Minatec, 2STMicroelectronics, Grenoble, France (invited talk)

3:30pm  4.2  Design Challenges and Solutions for Ultra-High-Density Monolithic 3D ICs  32
S. Panth¹, S. Samal¹, Y.S. Yu², and S.K. Lim¹; ¹Dept. of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, USA, ²Hankyong National University, Korea (invited talk)

4:00pm  4.3  3D Memory with Shared Lithography Steps: The Memory Industry’s Plan to “Cram More Components onto Integrated Circuits”
D. C. Sekar, Rambus Labs (invited talk)

4:30pm  4.4  Monolithic 3D Integration in a CMOS Process Flow  37
E.A. Fitzgerald¹ ², S.F. Yoon¹ ³, C.S. Tan¹ ², T. Palacios¹ ², X. Zhou¹ ², L.S. Peh¹ ², C.C. Boon¹ ², D.A. Kohen³, K.H. Lee³, Z.H. Liu³, P. Cho³ ³; ¹Low Energy Electronic Systems, SMART Singapore, ²Massachusetts Institute of Technology Cambridge, MA, ³Nanyang Technological University, Singapore (invited talk)

5:00pm  4.5  Monolithic 3D Integration Advances and Challenges: From Technology to System Levels
M.S. Ebrahimi, G. Hills, M.M. Sabry, M. M. Shulaker, H. Wei, T.F. Wu, S. Mitra, H.-S. Philip Wong; Department of Electrical Engineering and Department of Computer Science, Stanford University (invited talk)

2014 IEEE S3S Conference | Millbrae, CA
SESSION 5:
Joint Poster Session and Reception
5:30 to 7:30pm
Poplar / Westin Ballroom Foyer

SESSION CHAIR
Chang-Lee Chen, MIT Lincoln Laboratory

5.1 Performance Assessment of ULP Analog/RF MOSFET Architectures
D. Ghosh, A. Kranti; Low Power Nanoelectronics Research Group, Electrical Engineering Discipline, Indian Institute of Technology, Indore, India

5.2 On the Cryogenic Performance of Ultra-Low-Loss, Wideband SPDT RF Switches Designed in a 180 nm SOI-CMOS Technology
A.S. Cardoso, P.S. Chakraborty, A.P. Omprakash, N. Karaulac, P. Saha, J.D. Cressler; School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA

5.3 Analog Performance of Short-Channel Asymmetric Self-Cascode of Junctionless Nanowire nMOS Transistors
M. de Souza, R.T. Doria, R.D. Trevisoli, M.A. Pavanello; Electrical Engineering Department, Centro Universitário da FEL, São Bernardo do Campo, Brazil

5.4 Multi-Threshold Design Methodology of Stacked Si-Nanowire FETs
Y.-B. Liao1, M.-H. Chiang2; 1Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan, 2MS Degree Program on Nano-IC Engineering, Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan

5.5 Analog Building Block Design in 14nm FinFET Using Inversion Coefficient
A. Wang, V. Dhawan, C.-J. R. Shi; Department of Electrical Engineering, University of Washington, Seattle WA, Supported by Semiconductor Research Corporation (SRC) under Task 1836.095 and the State of Washington Joint Center for Aerospace Technology Innovation (JCATI).

5.6 28 nm FD SOI Technology Platform RF FoM
B.K. Esfeh1, V. Klichytska1, V. Barra2, N. Planes3, M. Haond3, D. Flandre1, J.-P. Raskin1; 1ICTEAM, Université catholique de Louvain, Louvain-la-Neuve, Belgium, 2CEA-Leti, MINATEC Campus, Grenoble, France, 3ST-Microelectronics, Crolles, France

5.7 An SOI Based Integrated Gate-Drivers for Automotive Application
K. Toshiyuki, Y. Hiya, K. Kinoshita, H. Tomita, N. Hoshikawa; Electronics Development Div. 3 Toyota Motor Corporation, Toyota Aichi, Japan

5.8 Effect of Back Gate on Parasitic Bipolar Effect in FD SOI MOSFETs
F. Liu1, I. Ionica1, M. Bawedin2, S. Cristoloveanu1; 1IMEP-LAHC, MINATEC, Grenoble, France, 2Université Montpellier II, Montpellier, France

5.9 High Temperature Performance of Flexible SOI FinFETs with Sub-20 nm Fins
A. Diab, G.A. Torres Sevilla, M.T. Ghoneim, M.M. Hussain; Integrated Nanotechnology Lab, King Abdullah University of Science and Technology, Saudi Arabia
5.10 **Effects of Back-Gate Bias on Switched-Capacitor DC-DC Converters in UTBB FD-SOI**

M.J. Turnquist\(^1\), G. de Streel\(^3\), D. Bol\(^3\), M. Hiienkari\(^2\), L. Koskinen\(^2\); \(^1\)Dept. of Micro- and Nanosciences, Aalto University, \(^2\)University of Turku, Technology Research Center, \(^3\)ICTEAM Institute, Université catholique de Louvain

5.11 **An Optimal Probing Method of Pre-Bond TSV Fault Identification for 3D Stacked ICs**

B. Zhang, V.D. Agrawal; Department of Electrical and Computer Engineering, Auburn University, Auburn AL

5.12 **Power Supply Voltage Detection and Clamping Circuit for 3-D Integrated Circuits**

D. Pathak, I. Savidis; Department of Electrical and Computer Engineering, Drexel University, Philadelphia PA

5.13 **Study of Fin-Tunnel FETs with Doped Pocket as Capacitor-less 1T DRAM**

A. Biswas, A.M. Ionescu; ST-IEL-NANOLAB, Ecole Polytechnique Fédérale de Lausanne, Switzerland

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**SESSION 6A:**

**FDSOI**

**8:00am**

**Sequoia**

**SESSION CHAIRS**

Manfred Horstmann, Global Foundries ● Bich-Yen Nguyen, SOITEC

8:00am 6a.1 **UTBB/FDSOI: reasons for a success**

M. Haond, STMicroelectronics, Crolles, France (invited talk)

8:40am 6a.2 **Piezoresistivity in Unstrained and Strained SOI MOSFETs**

R. Berthelon\(^1\), M. Cassé\(^1\), D. Rideau\(^2\), O. Nier\(^1,2,3\), F. Andrieu\(^1\), E. Vincen\(^2\), G. Reimbold\(^1\); \(^1\)CEA-Leti, MINATEC Campus, Grenoble, France, \(^2\)STMicroelectronics, Crolles, France, \(^3\)IMEP-LAHC, MINATEC, Grenoble, France

9:00am 6a.3 **nFET FDSOI Activated by Low Temperature Solid Phase Epitaxial Regrowth: Optimization Guidelines**

L. Pasini\(^1,2,3\), P. Batude\(^1\), M. Cassé\(^1\), L. Brunet\(^1\), P. Rivallin\(^1\), B. Mathieu\(^1\), J. Lacord\(^1\), S. Martinie\(^1\), C. Fenouillet-Beranger\(^1\), B. Previtali\(^1\), N. Rambal\(^1\), M. Haond\(^2\), G. Ghibaudo\(^3\), M. Vinet\(^1\); \(^1\)CEA-Leti, MINATEC Campus, Grenoble, France, \(^2\)STMicroelectronics, Crolles, France, \(^3\)IMEP-LAHC, MINATEC/INPG, Grenoble, France

9:20am 6a.4 **In-depth Characterization of Hole Transport in 14nm FD-SOI pMOS Devices**

M. Shin\(^1,3\), M. Shl\(^1\), M. Mouis\(^1\), A. Cros\(^2\), E. Josse\(^2\), G.T. Kim\(^3\), G. Ghibaudo\(^1\); \(^1\)IMEP-LAHC, Grenoble INP, Minatec, Grenoble, France, \(^2\)STMicroelectronics, Crolles, France, \(^3\)School of Electrical Engineering, Korea University, Seoul, South Korea
SESSION 6B:
SubVt-Low Voltage Devices 1

8:00am
Redwood

SESSION CHAIR
Dan Radak, IDA

8:00am  6b.1  Spin-Transfer-Torque Devices for Boolean and Non-Boolean Computing
K. Roy, Purdue University (invited talk)

8:40am  6b.2  Near-0.1V Ultra-low Voltage Operation of SOTB 1M Logic Gates
Y. Ogasahara, M. Hioki, T. Nakagawa, T. Sekigawa, T. Tsutsumi, H. Koike; Nanoelectronics Research Institute, AIST, Tsukuba, Japan

9:00am  6b.3  Performance Prediction for Multiple-Threshold 7nm-FinFET-Based Circuits Operating in Multiple Voltage Regimes Using a Cross-Layer Simulation Framework
S. Chen, Y. Wang, X. Lin, Q. Xie, M. Pedram; University of Southern California, CA, USA

9:20am  6b.4  A Cross-Layer Design Framework and Comparative Analysis of SRAM Cells and Cache Memories using 7nm FinFET Devices
A. Shafaei, S. Chen, Y. Wang and M. Pedram; Department of Electrical Engineering, University of Southern California, Los Angeles, CA, USA

9:40am  6b.5  Efficient Ultra Low Power Rectification at 13.56 MHz for a 10 μA Load Current
P.-A. Haddad, G. Gosset, J.-P. Raskin and D. Flandre; Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM), Université catholique de Louvain, Louvain-la-Neuve, Belgium
SESSION 7A:
SOI Circuit Design
10:20am
Sequoia

SESSION CHAIRS
Toshiro Hiramoto, University of Tokyo ● Francisco Gamiz, University of Granada

10:20am  7a.1  FDSOI Circuit Design for a Better Energy Efficiency  N/A
E. Beigné, CEA-Leti (invited talk)

11:00am  7a.2  Experimental Model of Adaptive Body Biasing for Energy Efficiency  94
in 28nm UTBB FD-SOI
M. Cochet1,2, B. Pelloux-Prayer1, M. Saligane1,2,3, S. Clerc1, P. Roche1, J.-L. Autran2,
D. Sylvester3; 1STMicroelectronics, Crolles, France, 2IM2NP – Aix-Marseille University,
France, 3University of Michigan, Ann Arbor, MI

11:20am  7a.3  UTBB FD-SOI Front- and Back-Gate Coupling Aware Random  96
Telegraph Signal Impact Analysis on a 6T SRAM
K.C Akyel1,3, L.Ciampolini1, O. Thomas2, D.Turgis1, G.Ghibaudo3; 1STMicroelectronics,
Crolles, France, 2CEA-Leti Campus Minatec, Grenoble, France, 3IMEP-LAHC, Minatec,
Grenoble, France

11:40am  7a.4  Mixed-Single Well 8T SRAM Bitcell for Wide Voltage Range in 28nm  98
FDSOI
A. Makosiej1, N. Planes2, R. Ranica2, L. Ciampolini2 and O. Thomas1;
1Univ. Grenoble Alpes; CEA-Leti, MINATEC Campus, Grenoble, France,
2STMicroelectronics, Crolles, France

SESSION 7B:
SubVt – Low Voltage Devices 2
10:20am
Redwood

SESSION CHAIR
Paul Franzon, North Carolina State University

10:20am  7b.1  The Center for Energy Efficient Electronics Science: the Search for  N/A
Really Low Threshold Voltage
E. Yablonovitch, UC Berkeley (invited talk)

2014 IEEE S3S Conference | Millbrae, CA
SESSION 8A:
Novel SOI Structures

8:00am
Sequoia

SESSION CHAIR
Philippe Flatresse, STMicroelectronics

8:00am  8a.1  Electron-Hole Bilayer Deep Subthermal Electronic Switch: Physics, Promise and Challenges  106
A.M. Ionescu1, C. Alperi1, J.L. Padilla1, L. Lattanzio1, P. Palestri2;1NANOLAB, Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland, 2DIEGM, University of Udine, Udine, Italy (invited)

8:40am  8a.2  Beyond TFET: Alternative Mechanisms for SMOS -Compatible Sharp- Switching Devices  109
S. Cristoloveanu; IMEP-LAHC (invited)

9:20am  8a.3  A2RAM: Low-power 1T-DRAM Memory Cells Compatible with Planar and 3D SOI Substrates  111
F.Gamiz1, N.Rodriguez1, C.Marquez1, C.Navarro2 and S.Cristoloveanu2; 1Nanoelectronics Laboratory, Department of Electronics, University of Granada, Granada Spain, 2IMEP, Grenoble INP MINATEC, Grenoble, France (invited)
SESSION 8B: SubVt – Energy Harvesting for Low Power Circuits

8:00am Redwood

SESSION CHAIR
Dennis Buss, Texas Instruments

8:00am  8b.1 Ultra Low Voltage Energy Harvesting: Challenges and Design Methodologies
S. Mukhopadhyay, Georgia Tech (invited talk)

8:40am  8b.2 Bias-Flip Technique for Frequency Tuning of Piezo-Electric Energy Harvesting Devices: Experimental Verification
S. Zhao¹, Y. Ramadass², J.H. Lang³, J. Ma¹, D. Buss²,³; ¹Tianjin University, School of Electronic Information Engineering, Tianjin, P.R. China, ²Texas Instruments, Inc., Dallas, TX, USA, ³Massachusetts Institute of Technology, EECS Dept. Cambridge, MA, USA

9:00am  8b.3 Adaptive Subthreshold Switched Capacitor Voltage Boost for Thermoelectric Generation
R. Brito¹, M. Barba¹, P. Palakurthi¹, D. Nemir²; E. MacDonald¹; ¹Electrical and Computer Engineering, University of Texas at El Paso, El Paso, Texas, USA, ²TXL Group, Inc., El Paso, Texas, USA

9:20am  8b.4 Subthreshold RF Powered Digital Circuits
P.D. Franzon, P. Gadfort, J. Schabel, W. Xu; North Carolina State University (invited talk)

SESSION 9A: SOI Substrates

10:20am Sequoia

SESSION CHAIRS
Sorin Cristoloveanu, IMEP ● Frederic Allibert, SOITEC

10:20am  9a.1 SOI Substrate Solutions for Recent Advanced Device Applications
<table>
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<th>Time</th>
<th>Session</th>
<th>Title</th>
<th>Authors</th>
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<tbody>
<tr>
<td>11:00am</td>
<td>9a.2</td>
<td>The Role of Radiation Effects in SOI Technology Development</td>
<td>L. Palkuti¹, M. Alles², H. Hughes³; ¹Defense Threat Reduction Agency, Ft Belvoir, VA, ²Vanderbilt University, Nashville, TN, ³Naval Research Laboratory, Washington, DC (invited talk)</td>
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<tr>
<td>11:20am</td>
<td>9a.3</td>
<td>A Very Low Power CMOS 28FDSOI Programmable Fractional Frequency Divider for Wifi-WiGig</td>
<td>M. Vallet¹, O. Richard¹, Y. Deval², D. Belot¹; ¹STMicroelectronics, Crolles, France, ²IMS Bordeaux, Talence, France</td>
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<tr>
<td>11:40am</td>
<td>9a.4</td>
<td>Recent Advances and Future Trends in SOI for RF Applications</td>
<td>A. Joshi, T.-Y. Lee, Y.-Y. Chen and D. Whitefield; Skyworks Solutions Inc. Irvine, CA (invited talk)</td>
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### SESSION 9B:
SubVt – Radiation Effects on Low Voltage Circuits and Late News

**10:20am**
Redwood

**SESSION CHAIR**
Lew Cohn, NRO

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<th>Time</th>
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<th>Authors</th>
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<tr>
<td>10:20am</td>
<td>9b.1</td>
<td>SEU Hardening: Incorporating an Extreme Low Power Bitcell Design (SHIELD)</td>
<td>A. Pescovsky¹, O. Chertkow¹, L. Atlas¹, A. Fish²; ¹VLSI Systems Center, Ben-Gurion University of the Negev, Be’er Sheva, ²Faculty of Engineering, Bar-Ilan University, Ramat Gan</td>
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<tr>
<td>10:40am</td>
<td>9b.2</td>
<td>Impact of Ultra-Low Voltages on Single-Event Transients and Pulse Quenching</td>
<td>J.R. Ahlbin, P. Gadfort; Information Sciences Institute, University of Southern California, Arlington, VA</td>
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<tr>
<td>11:00am</td>
<td>9b.3</td>
<td>Compensation of Total Ionizing Dose Effects in ULV SoCs through Adaptive Voltage Scaling</td>
<td>J. De Vos, V. Kilchytska, D. Flandre, D. Bol; ICTEAM Institute, Université catholique de Louvain (UCL) Louvain-la-Neuve, Belgium</td>
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<tr>
<td>11:20am</td>
<td>9b.4</td>
<td>Near-Threshold Voltage Operation of Nonvolatile SRAM Cell Based on Pseudo-Spin-FinFET Architecture</td>
<td>Y. Shuto, S. Yamamoto, S. Sugahara; Imaging Science and Engineering Laboratory, Tokyo Institute of Technology, Yokohama, Japan</td>
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</table>
More than an Order of Magnitude Energy Improvement of FPGA by Combining 0.4V Operation and Multi-Vt Optimization of 20k Body Bias Domains
H. Koike1, C. Ma1,2, M. Hioki1, Y. Ogasahara1, T. Tsutsumi2, T. Nakagawa1, T. Sekigawa1; 1National Institute of AIST, 2Meiji University, Japan

SESSION 10:
Special Invited MEMS Hot Topics
1:00pm
Sequoia

SESSION CHAIR
Jeremy Muldavin, MIT Lincoln Laboratory

1:00pm 10.1 Inertial MEMS using SOI N/A
B. Taheri, Freescale (invited talk)

1:20pm 10.2 Si Resonators and MEMS using SOI N/A
T. Kenney, Stanford (invited talk)

1:40pm 10.3 SOI Wafer Manufacturing for MEMS N/A
A. Cornell, Okmetic (invited talk)

2:00pm 10.4 SOI Based Inertial Sensors N/A
A. Shkel, UCI (invited talk)

SESSION 11:
3D New Developments
3:00pm
Sequoia

SESSION CHAIR
Olivier Faynot, CEA-Leti

3:00pm 11.1 Monolithic IC Integration Key Alignment Aspects for High Process Yield 140
T. Uhrmann, T. Wagenleitner, T. Glisner, M. Wimlinger, P. Linder; EV Group, St. Florian am Inn, Austria
SESSION 12:
Late News Session
4:20pm
Sequoia

SESSION CHAIR
Bruce Doris – IBM

4:20pm  12.1 **Smart Co-Integration of Light Sensitive Layers with FDSOI Transistors for More than Moore Applications**  

4:40pm  12.2 **Prototype of Multi-Stacked Memory Wafers Using Low-Temperature Oxide Bonding and Ultra-Fine-Dimension Copper Through-Silicon Via Interconnects**  
W. Lin1, J.Faltermeyer1, K. Winstell1, S. Skordas1, T. Graves-Abe2, P. Batra2, K. Herman2, J. Golz2, T. Kirihata2, J. Garant2, A. Hubbard1, K. Cauffman1, T. Levine1, J. Kelly1, D. Priyadarshini1, B. Peethalai1, R. Pattolla1, M. Shoudy1, J.J. Demarest1, J. Wynne1, D. Canaperi1, D. McHerron1, D. Berger2, S. Iyer2; IBM Corporation Systems and Technology Group, 1Albany, NY, 2Hopewell Junction, NY

5:00pm  12.3 **A 262nW Analog Front End with a Digitally-Assisted Low Noise Amplifier for Batteryless EEG Acquisition**  
P. Bhargava1, W. D. Hairston2, R. M. Proie1; 1U.S. Army Research Laboratory Sensors and Electron Devices Directorate, 2Human Research and Engineering Directorate