
Amsterdam, Netherlands
4 – 9 October 2015
1.1 - Embedded System and Application Aware Design of Deregulated Energy Delivery Systems  
Robert Dick, Xuejing He, Russ Joseph

1.2 - Optimizing Mobile Display Brightness by Leveraging Human Visual Perception  
Matthew Schuchhardt, Susmit Jha, Raid Ayoub, Michael Kishinevsky, Gokhan Memik

1.3 - QuadSeal: Quadruple Algorithmic Symmetrizing Countermeasure Against Power Based Side-channel Attacks  
Darshana Jayasinghe, Aleksandar Ignjatovic, Jude Angelo Ambrose, Roshan Ragel, Sri Parameswaran

2.1 - Approximate Acceleration: A Path through the Era of Dark Silicon and Big Data  
Hadi Esmaeilzadeh

2.2 - Does Customizing Inexactness Help Over Simplistic Precision (bit-width) Reduction? A Case Study  
John Augustine, Ashutosh Ingole, Biswaroop Maiti, Krishna Palem

2.3 - Energy-interference-free System and Toolchain Support for Energy-harvesting Devices  
Brandon Lucia, Alexei Colin, Alanson Sample

2.4 - Accuracy-Aware Optimization of Approximate Programs  
Sasa Misailovic

3.1 - Evaluating and Exploiting Impacts of Dynamic Power Management Schemes on System Reliability  
Puneet Gupta, Liangzhen Lai, Vikas Chandra

3.2 - Exploiting Cache Conflicts to Reduce Radiation Sensitivity of Operating Systems on Embedded Systems  
Paolo Rech, Thiago Santini, Luigi Carro, Flavio Rech Wagner

3.3 - Optimization of Multi-Channel BCH Error Decoding for Common Cases  
Russ Dill, Aviral Shrivastava, Hyunok Oh

4.1 - Program Analysis for Approximation-aware Compilation  
Pooja Roy, Jianxing Wang, Weng Fai Wong

4.2 - Approximation-Aware Multi-Level Cells STT-RAM Cache Architecture  
Felipe Sampaio, Muhammad Shafique, Bruno Zatt, Sergio Bampi, Jörg Henkel

4.3 - Quality-Aware Data Allocation in Approximate DRAM  
Arnab Raha, Hrishikesh Jayakumar, Soubhagya Sutar, Vijay Raghunathan

5.1 - Vector-Aware Register Allocation for GPU Shader Processors  
Yi-Ping You, Szu-Chieh Chen
5.2 - A Sparse Matrix Vector Multiply Accelerator for Support Vector Machine 109
Eriko Nurvitadhi, Asit Mishra, Debbie Marr

5.3 - Saving Memory Movements Through Vector Processing in the DRAM 117
Luigi Carro, Marco Antonio Zanata Alves, Paulo Santos, Francis Birck Moreira, Matthias Diener

6.1 - Efficient SAT-based Application Mapping and Scheduling on Multiprocessor Systems for Throughput Maximization 127
Weichen Liu, Zonghua Gu, Yaoyao Ye

6.2 - NUVA: Architectural Support for Runtime Verification of Parametric Specifications over Multicores 137
Ahmed Nassar, Fadi Kurdahi, Wael Elsharkasy

6.3 - High Performance and Energy Efficient Wireless NoC-Enabled Multicore Architecture for Graph Analytics 147
Partha Pande, Karthi Duraisamy, Hao Lu, Ananth Kalyanaraman

7.1 - Timing Characterization of OpenMP4 Tasking Model 157
Eduardo Quinones, Maria A. Serrano, Alessandra Melani, Roberto Vargas, Andrea Marongiu, Marko Bertogna

7.2 - Scheduling Instruction Effects for a Statically Pipelined Processor 167
Magnus Sjalander, Brandon Davis, Peter Gavin, Ryan Baird, Ian Finlayson, Farhad Rasapour, Gregory Cook, Gang-Ryung Uh, David Whalley, Gary Tyson

7.3 - Reducing Shift Penalty in Domain Wall Memory through Register Locality 177
Ehsan Atoofian

8.1 - Self-Powered Wearable Sensor Platforms for Wellness 187
Veena Misra, John Lach, Alper Bozkurt, Benton Calhoun, David Wentzloff, Suman Datta, Vijay Narayanan, Omer Oralkan, Mehmet Ozturk, Jason Strohmaier

8.2 - Cognitive Cameras: Assistive Vision Systems 188
Kevin Irick, Vijaykrishnan Narayanan, Jack Sampon, Peter Zientra

8.3 - Self-powered Wearable Sensor Node: Challenges and Opportunities 189
Yougpan Liu, Hehe Li, Zewei Li, Xueqing Li, Kaisheng Ma, Jason Chun, Sampson John, Yuan Xie, Huazhong Yang