
Oslo, Norway
26-28 October 2015
Tuesday 27 October

1. Opening

09.15 Invited talk: Title TBD
Ivo Bolsens, Xilinx, US

10.00 Long-Term ECG Monitoring with Zeroing Compressed Sensing Approach 171
Mangia, Mauro; Bortolotti, Daniele; Bartolini, Andrea; Pareschi, Fabio; Benini, Luca; Rovatti, Riccardo; Setti, Gianluca, University of Bologna, IT

10.20 Digital Background Calibration in Continuous-time Delta-Sigma Analog to Digital Converters 104
Tan, Siyu; Miao, Yun; Palm, Mattias; Rodrigues, Joachim; Andreani, Pietro, Lund University, SE

2.1 Data Converters

11.10 A 10-bit Reference Free Current Mode SAR ADC with 58.4 dB SFDR at 50 MS/s in 90 nm CMOS 5
Elkafrawy, Abdelrahman; Anders, Jens; Ortmanns, Maurits, University of Ulm, DE

11.50 Fundamental Power Limits of SAR and ΔΣ Analog-to-Digital Converters 143
Brenna, Stefano; Bettini, Luca; Bonfanti, Andrea; Lacaita, Andrea Leonardo, Politecnico di Milano, IT

12.10 A Fully Synthesized All-Digital VCO-Based Analog-to-Digital Converter 139
Vishnu Unnikrishnan, Srinivasa Rao Pathapati and Mark Vesterbacka, Linköping University, SE

12.30 System Level Design of a Continuous-Time ΔΣ Modulator for Portable Ultrasound Scanners 231
Llimos Muntal, Pere; Færch, Kjartan; Jørgensen, Ivan H.H.; Bruun, Erik, Technical University of Denmark, DK

2.2 Reconfigurable Architectures

11.10 Executing Secured Virtual Machines within a Manycore Architecture 115
Dévigne, Clément; Bréjon, Jean-Baptiste; Meunier, Quentin; Wajsburt, Franck, Université Pierre et Marie Curie, FR

11.30 Design, Implementation and Analysis of a Reconfigurable Memory Management Unit on FPGA 88
Shamani, Farid; Fukouv Sevom, Vida; Nurmi, Jari; Ahonen, Tapani, Tampere University of Technology, FI

11.50 Empirical Results on Parity-based Soft Error Detection with Software-based Retry 108
Aydos, Gökçe; Fey, Görschwin, University of Bremen, DE

12.10 Fault Tolerant Field Programmable Neural Networks 119
Krčma, Martin; Kotásek, Zdeněk; Kaštil, Jan, Faculty of Information Technology, Brno University of Technology, CZ

12.30 Secured-by-Design FPGA: Look-Up Tables and Switch-Boxes 211
Almohainid, Ziad; Sima, Mihai, University of Victoria, CA

3.1 PLLs

14.00 A BW-tracking semi-digital PLL with near-optimal VCO phase noise shaping in low-cost 0.4 μm CMOS achieving 700 fs rms phase jitter 13
Fahmy, Said; Sareen, Puneet; Dietl, Markus; Ortmanns, Maurits; Anders, Jens, University of Ulm, DE

14.20 A 65nm CMOS Fraction-N Digital PLL with Shaped Inband Phase noise 9
Mahmoud, Ahmed; Andreani, Pietro; Lu, Ping, Lund University, SE
3.2 Communication Technology

14.00 Carrier Frequency and Sampling Rate Offsets Effect on Sub 6 GHz Massive MIMO
Ahmed-Ouameur, Messaoud; Massicotte, Daniel; Zhu, Wai-Ping, Universite du Quebec a Trois-Rivieres, CA

14.20 Parallel Independent FFTs Implementation on Intel Processors and Xeon Phi for LTE and OFDM Systems
Khelifi, Mounir; Massicotte, Daniel; Savaria, Yvon, Université du Québec à Trois-Rivières, CA

14.40 Two-Variable Numeric Function Approximation Using Least-Squares-Based Regression
Rust, Jochen; Heidmann, Nils; Paul, Steffen, University of Bremen, DE

4. Poster session I

Analog circuits

Ultra low-power, -area and -frequency CMOS thyristor based oscillator for autonomous microsystems
Funke, Dominic Alexander; Oehm, Jürgen; Mayr, Pierre; Maeke, Thomas; McCaskill, John Simpson; Sharma, Abhishek; Straczek, Lukas, Ruhr Universität Bochum, DE

Analysis and Design of a 1.1dB-IL third-order Matching Network for Switched-Capacitor PAs
Passamani, Antonio; Ponton, Davide; Knoblinger, Gerhard; Bevilacqua, Andrea, University of Padova, IT

A New Current Stimulator Architecture for Visual Cortex Stimulation
Osipov, Dmitry; Paul, Steffen; Strokov, Serge; Kreiter, Andreas K., University of Bremen, DE

A CMOS High Resolution Multi-Edge Delay Generator
Harb, Shadi; Eisenstadt, William, Intel Corporation, US

A Capacitor-Free, Fast Transient Response Linear Voltage Regulator In a 180nm CMOS
Deleuran, Alexander Nymann; Lindbjerg, Nicklas; Pedersen, Martin Kofoed; Llimós Muntal, Pere; Jørgensen, Ivan Harald Holger, Technical University of Denmark, DK

Single Chip Wireless Condition Monitoring of Power Semiconductor Modules
Nilsson, Joakim; Borg, Johan; Johansson, Jonny, Luleå University of Technology, SE

Ultra Low Power On-Chip Hybrid Start-Up for Wireless Sensor Networks
Vamsi, Nagaveni; Gupta, Akash; Dutta, Ashudeb; Singh, Shiv Govind, Indian Institute of Technology Hyderabad, IN

Full Swing 20 GHz Frequency Divider with 1 V Supply Voltage in FD-SOI 28 nm Technology
Ozsema, Hasene Gulperi; Kostak, Duylgu; Demirci, Tugba; Leblebici, Yusuf, Swiss Federal Institute of Technology Lausanne (EPFL), CH

System-on-Chip

A Hardware Architecture for the Branch and Bound Flow-Shop Scheduling Algorithm
Daouri, Mikhael; Escobar Juzga, Fernando Adolfo; Chang, Xin; Valderrama, Carlos, UMONS, BE

Interfacing Hardware Accelerators to a Time-Division Multiplexing Network-on-Chip
Pezzarossa, Luca; Sørensen, Rasmus Bo; Shoeberl, Martin; Sparso, Jens, Technical University of Denmark, DK

Design of a Hybrid Multicore Platform for High Performance Reconfigurable Computing
Hussain, Waqar; Hoffmann, Henry; Ahonen, Tapani; Nurmi, Jari, Tampere University of Technology, FI

How Small and Still Effective a CMOS-SoC Could ever be?
Heusala, Hannu H.; Skytta, Jorma, Aalto University, FI
5.1 DC/DC converters

15.50 High-Efficiency Peak-Current-Control Non-inverting Buck-Boost Converter Using Mode Selection for Single Ni-MH Cell Battery Operation 147
Kim, Jong-Seok; Lee, Jae-Yoon; Choi, Byong-Deok, Hanyang University, KR

16.10 Application of spread-spectrum techniques to class-E DC/DC converters: some preliminary results 57
Pareschi, Fabio; Vincenzi, Tommaso; Mangia, Mauro; Berton, Nicola; Rovatti, Riccardo; Setti, Gianluca, University of Ferrara, IT

5.2 Digital System Design

15.50 Fault-Tolerant Implementation of Direct FIR Filters Protected Using Residue Codes 123
Piestrak, Stanislaw; Patronik, Piotr, Wroclaw Univ. of Technology, PL

16.10 Low Power Unrolled CORDIC Architectures 179
Nilsson, Peter (1); Gangarajaiah, Rakesh (1); Sun, Yuhang (1); Hertz, Erik (2), 1 Lund University, 2 Halmstad University

16.30 Invited talk: The electronics industry is suffering from bad priorities in the university education
Espen Tallaksen, Bitvis, Norway

Wednesday 28 October

09.00 Invited talk: Design Challenges for the Internet of Things
Danielle Griffith, TI, US

6. Poster session II

Digital systems

Formal Analysis of Macro Synchronous Micro Asynchronous Pipeline for Hardware Trojan Detection 131
Lodhi, Faiq Khalid; Hasan, Syed Rafay; Hasan, Osman; Awwad, Falah, National University of Sciences and Technology, PK

An Ultra-Low-Power/High-Speed 9-bit Adder Design: Analysis and Comparison Vs. Technology from 130nm-LP to UTBBF-SOI-28nm 49
Atarzadeh, Hourieh; Aunet, Snorre; Yttredal, Trond, Norwegian University of Science and Technology, NO

The Low Delay Low-Pass FIR Digital Differentiators Having Flat Passband and Equiripple Stopband 239
Yoshida, Takashi; Aikawa, Naoyuki, Tokyo University of Science, JP

Architectural Design Space Exploration of an FPGA-based Compressed Sampling Engine: Application to Wireless Heart-Rate Monitoring 61
El-Sayed, Mohammad; Koch, Peter; Le Moullec, Yannick, Tallinn University of Technology, EE

A design platform for flexible programmable DSP for automotive sensor conditioning 33
Sisto, Arcangelo; Pilato, Luca; Serventi, Riccardo; Fanucci, Luca, University of Pisa, IT

Analog circuits

Wide band edge-coupled impedance matching network with quarter wavelength measurement circuit 263
Yadegar Amin, Hamid; Yarman, binboğa Siddik, Istanbul Technical University, TU

Self-Biasing High-Voltage Driver Based on Standard CMOS with an Adapted Level Shifter for a Wide Range of Supply Voltages 215
Pashmineh, Sara; Killat, Dirk, Brandenburg University of Technology, DE
An Ultra Wide-Band Adaptive Frequency Divider For mm-wave PLL Applications 53
Athanasiadis, Pavlos; Mountrichas, Lampros; Siskos, Stylianos, Aristotle University of Thessaloniki, GR

A Low/High Band Highly Linearized Reconfigurable Down Conversion Mixer in 65nm CMOS Process 41
Gupta, Nisha; Dutta, Ashudeb; Singh, Shiv Govind, IIT Hyderabad, IN

Fixed pattern noise correction for wide dynamic range CMOS image sensor with Reinhard tone mapping Operator 127
Mughal, Waqas; Choubey, Bhaskar, University of Glasgow, UK

Evaluation of the Vertical Magnetic Field Generated by a Spiral Planar Coil 112
Minnaert, Ben; Stevens, Nobby, KU Leuven, BE

Systematic frequency planning for a high SFDR digital-IF RF-DAC based transmitter 227
Hanay, Oner; Bayram, Erkan; Elsayed, Mohamed Saeed; Negra, Renato, RWTH Aachen University, DE

Design of a Highly Linear, Low Noise, Broad Band UpConverter for Cognitive Radio Applications 167
Varga, Gabor; Ashok, Arun; Subbiah, Iyappan; Schrey, Moritz; Heinen, Stefan, RWTH Aachen University, DE

A Noise Coupled ΣΔ Architecture using a Non Uniform Quantizer 195
Torreño Carrera, Juan Antonio; Patón Álvarez, Susana; Conesa-Peraleja, Laura; Straeussnigg, Dietmar; Hernández, Luis, Carlos III University Madrid, ES

6.1 “Mixed Analog”

10.30 A NAND Gate Based Standard Cell VCO for Use in Synthesizable ADCs 187
Unnikrishnan, Vishnu; Vesterbacka, Mark, Linköping University, SE

10.50 Process Tolerant Highly Linear Mixer Output Stage with Feedforward Linearity Improvement Method for a High-IF Converter 207
Ashok, Arun; Varga, Gabor; Subbiah, Iyappan; Schrey, Moritz; Heinen, Stefan, RWTH Aachen University, DE

11.10 On-Chip Spatial Filter for Subretinal Implants 199
Rieger, Viola; Schütz, Henning; Gambach, Stefan; Rothermel, Albrecht, University of Ulm, DE

6.2 Modeling and simulation of embedded systems

10.30 Design and Evaluation of Correlation Accelerator in IEEE-802.11a/g Receiver using a Template-based Coarse-Grained Reconfigurable Array 82
Nouri, Sajjad; Hussain, Waqar; Nurmi, Jari, Tampere University of Technology, FI

10.50 Test-Driven Modeling of Embedded Systems 235
Munck, Allan; Madsen, Jan, Technical University of Denmark, DK

11.10 Shared Structurally Synthesized BDDs for Speeding-Up Parallel Pattern Simulation in Digital Circuits 219
Ubar, Raimund Johannes; Jürimägi, Lembit; Raik, Jaan, Tallinn University of Technology, EE

7.1 Amplifiers

12.30 Highly linear and reliable low band class-O RF power amplifier in 130 nm CMOS technology for 4G LTE applications 151
Khan, Muhammad Abdullah; Farouk Aref, Ahmed; Wei, Muh Dey; Negra, Renato, RWTH Aachen University, DE

12.50 A compact 0.3-10 GHz Broadband Stacked Amplifier in 65nm standard CMOS 25
Tarar, Mohsin Mumtaz; Wei, Muh-Dey; Negra, Renato, RWTH Aachen University, DE

13.10 An Ultra-Low-Voltage OTA in 28 nm UTBB FDSOI CMOS Using Forward Body Bias 259
Harikumar, Prakash; Wikner, J Jacob; Alvandpour, Atila, Linköping University, SE

13.30 Low power, highly stable and wideband LNA for GNSS applications in SiGe technology 175
Deo, Navneeta; Wernehag, Johan; Thelberg, Joakim, Lund University, SE
7.2 Low Power Systems

12.30 A Comparison of Serial Interfaces on Energy Critical Systems
Solheim, Tharald; Grannæs, Marius, Silicon Labs, NO

12.50 Adaptive Power Monitoring For Self-aware Embedded Systems
El ahmad, Mohamad; Najem, Mohamad; Benoit, Pascal; Sassatelli, Gilles; Torres, Lionel, University of Montpellier, FR

13.10 Area and power savings via buffer reorganization in asymmetric 3D-NoCs for heterogeneous 3D-SoCs
Joseph, Jan Moritz; Blochwitz, Christopher; Garcia-Ortiz, Alberto; Pionteck, Thilo, Universität zu Lübeck, DE

13.30 Comparative Analysis of Flip-Flop Architectures for Subthreshold Applications in 28nm FDSOI
Låte, Even, Vatanjou, Ali Asghar, Ytterdal, Trond, Aunet, Snorre, NTNU, NO

13.50 Microcontroller Energy Consumption Estimation Based on Software Analysis for Embedded Systems
Ruberg, Priit; Lass, Keijo; Ellerbee, Peeter, Tallinn University of Technology, EE

Svein-Erik Hamran, Norwegian Defence Research Est./University of Oslo, NO