ICICDT 2016 Contributed and Invited Papers

Keynote

Tuesday, June 28th, 2016

8:30 AM  Keynote 1-Low Power CPU: from Mobile to Wearable & IoT, Uming Ko, MediaTek, USA

Session A: Low-Power Circuits & Technology

Tuesday, June 28th, 2016

Session Chair: Tran Xuan Tu

9:15 AM  A High-Throughput and Low-Power Design for Bitmap Indexing on 65-nm SOTB CMOS Process, Xuan-Thuan Nguyen, Hong-Thu Nguyen, and Cong-Kha Pham, The University of Electro-Communications, Tokyo, Japan.

9:25 AM  Ultra Low-Power and Low-Energy 32-bit Datapath AES Architecture for IoT Applications, Duy-Hieu Bui(1); Diego Puschini(1); Simone Bacles-Min(1); Edith Beigné(1); Xuan-Tu Tran(2), 1: Université Grenoble Alpes, Grenoble, FRANCE, 2: VNU University of Engineering and Technology, Hanoi, Vietnam.

9:35 AM  A Compact, Low Power AES Core on 180nm CMOS Process, Van-Lan Dao; Van-Phuc Hoang; Anh-Thai Nguyen; Quy-Minh Le, Le Quy Don Technical University, Hanoi, Vietnam.

9:45 AM:  Register Grouping for Synthesis of Clock Gating Logic, Inhak Han(1); Jonggyu Kim(2); Joonhwan Yi(2), Youngsoo Shin(1), 1: KAIST, Daejeon, Korea, 2: University of Kwangwoon, Seoul, Korea.

Session B – Reliability and Soft Error

Tuesday, June 28th, 2016

Session Chairs: Koji Eriguchi and Yuichiro Mitani

10:10 AM: Invited - Layout Dependent BTI and HCI Degradation in Nano CMOS Technology: A New Time-Dependent LDE and Impacts on Circuit at End of Life, Ru Huang; Pengpeng Ren; Runsheng Wang, Peking University, Beijing, China.

10:20 AM: Accuracy of Quasi-Monte Carlo technique in Failure Probability Estimations, Michail Noltsis(1); Dimitrios Rodopoulos(2); Pieter Weckx(2); Francky Catthoor(2); Dimitrios Soudris(1), 1: National Technical University of Athens, Greece; 2: imec, Belgium.
10:30 AM: **An Area Compact Soft Error Resident Circuit for FPGA**, Motoki Amagasaki; Yuji Nakamura; Takuya Teraoka; Masahiro Iida; Toshinori Sueyoshi, *Kumamoto University*, Japan.


**Session C – I/O Circuits and ESD Protection**

**Tuesday, June 28th, 2016**

**Session Chairs: Lorenzo Cerati and Philippe Galy**

10:50 AM: **A Method Of Leakage Reduction And Slew-Rate Adjustment in 2 x VDD output Buffer For 28 nm CMOS Technology And Above**, Tsung-Yi Tsai; Yan-You Chou; Chua-Chin Wang, *National Sun Yat-Sen University, Taiwan, Republic of China*.

11:00 AM: **Preliminary results on TFET - Gated diode in thin silicon film for IO design & ESD protection in 28nm UTBB FD-SOI CMOS technology**, Philippe Galy(1); Sotirios Athanasiou(2), 1: STmicroelectronics, France; 2: STmicroelectronics, IMEP, France.

**Keynote 2:**

**Tuesday, June 28th, 2016**

1:05 PM  **Keynote 2- Accelerating the Sensing World through Imaging Evolution**, Yoshikazu Nitta, *Sony Semiconductor Solutions Corporation, Atsugi, Japan*

**Session D: Advanced Transistors / Materials and High Power / High Voltage**

**Tuesday, June 28th, 2016**

**Session Chairs: Bich-Yen Nguyen and Wenke Weinreich**

1:50 PM: **Invited - FDSOI Technology: Toward 0.3V CMOS Operation**, Olivier Webber, *STM, CEA-Leti, France*.

2:00 PM: **Extending HKMG scaling on CMOS with FDSOI: advantages and integration challenges**, Dina Triyoso(1); Rick Carter(1); Jon Kluth(1); Klaus Hempel(2); Michael Gribelyuk(1); Laegu Kang(1); Anil Kumar(1); Bob Mullfinger(1); Peter Javorka(2); Kasun Punchihewa(1); Amy Child(1); Tim McArule(1); Judson Holt(1); Ryan Sporer(1); Sherry Straub(1); Paul Chen(1), 1: GLOBALFOUNDRIES USA; 2: GLOBALFOUNDRIES Germany.

2:10 PM: **Characterization of High Pressure Hydrogen Annealing Effect on Polysilicon Channel Field Effect Transistors using Isothermal Deep Level Trap Spectroscopy**, Manh-Cuong Nguyen (1); An Hoang-Thuy Nguyen (1); Jae-Won Choi (1); Soo-Yeun Han (1); Jung-Yeon Kim(1); Rino Choi(1); Changhwan Choi(2), 1: Inha University, South Korea; 2: Hanyang University, South Korea.
2:20 PM: Invited - **Beyond-Si materials and devices for more Moore and more than Moore applications**, Nadine Collaert; A. Alian; H. Arimura; G. Boccardi; G. Eneman; J. Franco; Ts. Ivanov; D. Lin; J. Mitard; S. Ramesh; R. Rooyackers; M. Schaeckers; A. Sibaya-Hernandez; S. Sioncke; Q. Smets; A. Vais; A. Vandooren; A. Veloso; A. Verhulst; D. Verreke; N. Waldrong; A. Walke; L. Witters; H. Yu, X. Zhou; A. V.-Y. Thean, IMEC, Belgium.

2:30 PM: **Different Scalabilities of N- and P-Type Tunnel Field-Effect Transistors with Si/SiGe Heterojunctions**, Nguyen Dang Chien(1); Nguyen Thi Thu(2); Chun-Hsing Shih(3); Luu The Vinh(4), 1: Faculty of Physics, University of Dalat, Vietnam; 2: Department of Postgraduate Studies, University of Dalat, Vietnam; 3: National Chi Nan University, Taiwan, Republic of China; 4: Industrial University of Ho Chi Minh City, Vietnam.


2:50 PM: **On-chip Accurate Primary-side Output Current Estimator for Flyback LED Driver Control**, Chua-Chin Wang; Zong-You Hou; Teng-Wei Huang, National Sun Yat-Sen University, Taiwan, Republic of China.

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**Session E – RF&Analog Mixed Signal**

Tuesday, June 28th, 2016

**Session Chairs: Cuong Huynh and Dina Triyoso**

3:15 PM Invited - **An Assessment On Low-Voltage Low-Power Integrated Single Transistor Active Inductor Design for RF Filter Applications**, Vincenzo Stornelli, University of L’Aquila, Italy

3:25 PM **A 4.2 mW 3.1 dBm IIP3 LNA in 0.13 μm CMOS for Wideband Communications**, Benqing Guo; Jun Chen; Haiyan Jin, University of Electronic Science and Technology of China, People’s Republic of China.

3:35 PM **A 100-μW Wake-up Receiver for UHF Transceiver**, Phong Nguyen Thanh (1); Khanh Nguyen Tuan (2); Xuan Mai Dong (3,1,2): Integrated Circuit Design Research and Education Center (ICDREC), Vietnam National University, Vietnam; 3: Ho Chi Minh City University of Technology (HCMUT), Vietnam National University, Vietnam.

3:45 PM **A 65-nm CMOS High-Efficiency PWM/PFM Buck Converter with Bypass Mode for Transceiver Applications**, Duy Dang; Thang Tran Quoc; Kien Nguyen Van, Integrated Circuit Design Research and Education Center (ICDREC), Vietnam.

4:05 PM A 350uW 10-bit CMOS Cyclic D/A Converter with a Capacitor-Sharing Technique for Automatic Test Equipment, Youngcheol Son; Jiwhan Oh; Yongjun Cho; Hyundong Kim; Minkyu Song, Dongguk University, Seoul, Korea.

Conference Program

Keynote3

Wednesday, June 29th, 2016

8:15 AM Keynote3 - Microprocessor: Past, Present, and Future, Thang Tran, Synopsys Inc., USA

Session F – SoC/MPSoC/SIP & CAD/DFX

Wednesday, June 29th, 2016

Session Chairs: Dac Pham, Juergen Pille, and Rouwaida Kanj

9:00 AM Invited - Placement Optimization for MP-DSAI Compliant Layout, Seongbo Shim (1, 2); Woolhyun Chung (1); Youngsoo Shin (1); 1: Department of Electrical Engineering, KAIST, Daejeon 34101, Korea 2: Samsung Electronics, Hwasung 18448, Korea

9:10 AM A Digitally Controlled Oscillator Suitable for On-chip Integration in 65 nm CMOS, Shanthi Sudalaiyandi; Gilles Mason; Mykhailo Zarudniev, CEA LETI MINATEC, Grenoble, France.

9:20 AM The Implementation of Homeplug AV system, Ko-Chi Kuo, National Sun Yat-sen University, Taiwan, Republic of China.

9:30 AM Fast Design Exploration with Unified HW/SW co-verification Framework for High Throughput Wireless Communication System, Nana Sutisna (1); Reina Hongyo (1); Leonardo Lanante Jr.(2); Yuhei Nagao(2); Masayuki Kurosaki(2); Hiroshi Ochi(2), 1: Graduate School of Computer Science and Electronics, Kyushu Institute of Technology, Japan; 2: Department of Computer Science and Electronics, Kyushu Institute of Technology, Japan.

9:40 AM Routing-path Tracking and Updating Mechanism in Reconfigurable Network-on-Chips, Thi-Thuy Nguyen; Thanh-Vu Le-Van; Xuan-Tu Tran; Hung K. Nguyen, VNU University of Engineering and Technology (VNU-UET), Hanoi, Vietnam.

9:50 AM The Design of a Phase Compensator for The CIC Decimation Filter, Khanh Nguyen Quoc; Dong Bach Tuan; Toan Le Duc, Integrated Circuit Design Research and Education Center (ICDREC), Vietnam.

10:00 AM An All-in-One Debugger of 8-bit Microcontroller with High Transfer Speed, Nguyen Hung Quan; Duong Hai Dang Linh; Trinh Viet Quang; Hoang Minh The Nghi; Nguyen Phu Quoc; Tran Kien Cuong; Hoang Xuan Hoa, Integrated Circuit Design Research and Education Center (ICDREC), Vietnam.
Session G - Advanced Memory Devices

Wednesday, June 29th, 2016

Session Chair: Hideto Hidaka


10:40 AM Invited - Scaling of Split-Gate Flash Memory and its Adoption in Modern Embedded Non-Volatile Applications, Nhan Do, Microchip Technology Inc., USA.

10:50 AM An Ultra-Low Power Operated Logic NVM for Passive UHF RFID Tag Applications, Wu-Chang Chang; Po-Ching Wu; Cheng-Hao Po; Chun-Fu Lin; Ching-Yuan Lin; Chih-Hsin Chen, eMemory Technology Inc. Taiwan, Republic of China.

11:00 AM Dynamic CMOS-Rectifying memristor multiplier architecture for power reduction, Huan Minh Vo, Ho Chi Minh city University of Technology and Education, Vietnam.

11:10 AM 71% lossless compression of memory bandwidth for a multi-standard video codec by combination of 2D-DPCM and Variable Length Coding, Chi Lan Phuong Nguyen; My Phi Ngoc Nguyen; Hung Van Cao; Katsushige Matsubara; Keisuke Matsumoto; Seiji Mochizuki; Kenichi Iwata, 1: Renesas Design Vietnam Co., Ltd., Ho Chi Minh City, Vietnam, 2: Renesas System Design Co., Ltd., Tokyo, Japan.

Keynote4:

Wednesday, June 29th, 2016

1:20 PM Keynote4-Minimal Fab: a small semiconductor factory free from huge investment, Shiro Hara, AIST, Japan

Session H - Minimal Fab Application

Wednesday, June 29th, 2016

Session Chairs: Dang Luong Mo and Sommawan Khumpuang

2:05 PM Invited - Development of Fundamental Manufacturing Processes for Minimal Fab, Sommawan Khumpuang; Shiro Hara, National Institute of Advance Industrial Science and Technology (AIST).

2:15PM: Blue GaN based LED Fabrication using Hybrid Process of the Minimal Photolithography System and MOCVD, Masanori Iwata; Kenji Miyake; Nobuyoshi Yamauchi; Junko Kazusa, PMT Corporation, Fukuoka, Japan.
2:25 PM:  *Invited* - **Packaging in Minimal Fab**, Michihiro Inoue; Fumito Imura; Arami Saruwatri; Shiro Hara, *National Institute of Advance Industrial Science and Technology (AIST)*.

**Session I – 3D Integration & Emerging Technologies**

**Wednesday, June 29th, 2016**

**Session Chairs:** Thomas Ernst and Thuy Dao

2:55 PM  *Invited* - **Recent advances In 3D VLSI integration** Claire Fenouillet-Beranger; Maud Vinet, *CEA-Leti, France*.

3:05 PM  **La-doped ZrO2 based BEoL decoupling capacitors**, W. Weinreich (1); K. Seidel (1); P. Polakowski (1); M. Drescher (1), A. Gummenscheimer (2); M.G. Nolan (2); L. Cheng (3); D.H. Triyoso (3), 1: Fraunhofer IPMS-CNT, Dresden, Germany, 2: GLOBALFOUNDRIES, Dresden, Germany, 3: GLOBALFOUNDRIES, Malta, USA.

3:15 PM  *Invited* - **2.5D Interposer implementation**, Lisa Minwell, *eSilicon, USA*.


3:35 PM  **Exploration and Evaluation of Hybrid TFET-MOSFET Monolithic 3D SRAMs Considering Interlayer Coupling**, Jian-Hao Wang; Yin-Nien Chen; Pin Su; Ching-Te Chuang, *National Chiao Tung University, Taiwan, Republic of China*.

3:45 PM  **Conductive Polymer/Metal Composite for Flexible Interconnect**, Jin Kawakita; Toyohiro Chikyow, *National Institute for Materials Science, Japan*.