2016 International Great Lakes Symposium on VLSI (GLSVLSI 2016)

Boston, Massachusetts, USA
18-20 May 2016
# Table of Contents

GLSVLSI’16 Conference Organization ........................................................................................................... xiii

GLSVLSI’16 Sponsors and Supporters ............................................................................................................. xvii

## Keynote 1
Session Chair: Ayse Coskun (Boston University)
- **Why Is It So Hard to Make Secure Chips?** .......................................................... 1
  Marc Witteman (Riscure)

## Keynote 2
Session Chair: Jie Han (University of Alberta)
- **Design and Implementation of Real-Time Multi-sensor Vision Systems** ..................... 3
  Yusuf Leblebici (Swiss Federal Institute of Technology in Lausanne)

## Keynote 3
Session Chair: Martin Margala (University of Massachusetts, Lowell)
- **Medical Device Security: The First 165 Years** ............................................................... 5
  Kevin Fu (University of Michigan)

## Keynote 4
Session Chair: Laleh Behjat (University of Calgary)
- **VLSI Design Methods for Low Power Embedded Encryption** ...................................... 7
  Ingrid Verbauwhede (COSIC, KU Leuven AND UCLA)

### Session 1: VLSI Circuits 1
Session Chairs: Zain Navabi & (Worcester Polytechnic Institute), Swaroop Ghosh (University of South Florida)
- **High-Speed Polynomial Multiplier Architecture for Ring-LWE Based Public Key Cryptosystems** .................................................. 9
  Chaohui Du, Guoqiang Bai, Xingjun Wu (Tsinghua University)
- **Reduced Overhead Gate Level Logic Encryption** .......................................................... 15
  Kyle Juretus, Ioannis Savidis (Drexel University)
- **A Design of a Non-Volatile PMC-Based (Programmable Metallization Cell) Register File** 21
  Salin Junsangsri (Northeastern University), Jie Han (University of Alberta), Fabrizio Lombardi (Northeastern University)
- **A Clockless Sequential PUF with Autonomous Majority Voting** .................................. 27
  Xiaolin Xu, Daniel Holcomb (University of Massachusetts, Amherst)

### Session 2: VLSI and Test
Session Chair: Weikang Qian (Shanghai Jiaotong University)
- **Area-Efficient Error-Resilient Discrete Fourier Transformation Design using Stochastic Computing** .................................................. 33
  Bo Yuan (City University of New York, City College), Yanzhi Wang (Syracuse University), Zhongfeng Wang (Nanjing University)
- **Concurrent Error Detection for Reliable SHA-3 Design** ................................................. 39
  Pei Luo (Northeastern University), Cheng Li (University of Rochester), Yunsi Fei (Northeastern University)
- **Secure Model Checkers for Network-on-Chip (NoC) Architectures** ............................... 45
  Travis Boraten, Dominic DiTomaso, Avinash Karanth Kodi (Ohio University)
- **Parameter-importance based Monte-Carlo Technique for Variation-aware Analog Yield Optimization** ............................................. 51
  Sita kondamadugula, Srinath R. Naidu (International Institute of Information Technology, Bangalore)
Session 3: VLSI Design 1
Session Chairs: Himanshu Thapliyal & (University of Kentucky), Houman Homayoun (George Mason University)

- Low Energy Sketching Engines on Many-Core Platform for Big Data Acceleration ..........57
  Amey Kulkarni, Tahmid Abtahi, Emily Smith, Tinoosh Mohsenin (University of Maryland Baltimore County)

- Low-Power Manycore Accelerator for Personalized Biomedical Applications ..................63
  Adam Page, Nasrin Attaran, Colin Shea (University of Maryland, Baltimore County),
  Houman Homayoun (George Mason University), Tinoosh Mohsenin (University of Maryland, Baltimore County)

- Hardware Security Threats and Potential Countermeasures in Emerging 3D ICs ..............69
  Jaya Dofe, Qiaoqian Yu (University of New Hampshire), Hailang Wang. Emre Salman (Stony Brook University)

- Real-Time Analysis for Wormhole NoC: Revisited and Revised .................................75
  Qin Xiong (Huazhong University of Science and Technology), Zhonghai Lu (KTH Royal Institute of Technology),
  Fei Wu, Changsheng Xie (Huazhong University of Science and Technology)

Session 4: CAD 1
Session Chairs: Tosiron Adegbija (University of Arizona) & Marisa López-Vallejo (Universidad Politécnica de Madrid)

- A New Methodology for Noise Sensor Placement Based on Association Rule Mining .................................................................81
  Yu-Hsiang Hung, Sheng-Hsin Fang, Hung-Ming Chen (National Chiao Tung University),
  Shen-Min Chen, Chang-Tzu Lin, Chia-Hsin Lee (Industrial Technology Research Institute)

- MCFRoute 2.0 : A Redundant Via Insertion Enhanced Concurrent Detailed Router ................87
  Xiaotao Jia, Yici Cai, Qiang Zhou (Department of Computer Science and Technology, Tsinghua University),
  Bei Yu (CSE Department, The Chinese University of Hong Kong)

- Modular Placement for Interposer based Multi-FPGA Systems ......................................93
  Fubing Mao (Nanyang Technological University),
  Wei Zhang (Hong Kong University of Science and Technology),
  Bo Feng (Tsinghua University), Bingsheng He (Nanyang Technological University),
  Yuchun Ma (Tsinghua University)

- A Parallel Random Walk Solver for the Capacitance Calculation Problem in Touchscreen Design .................................................................99
  Zhezhao Xu, Wenjian Yu, Chao Zhang (Tsinghua University),
  Bolong Zhang (Tsinghua University & Florida State University), Meijuan Lu (Tsinghua University),
  Michael Mascagni (Florida State University)

Poster Session 1
Session Chair: Tali Moreshet (Boston University)

- Real-Time Hardware Stereo Matching Using Guided Image Filter ................................105
  Chen Yang, Yan Li, Wei Zhong, Song Chen (University of Science and Technology of China)

- Computing Complex Functions using Factorization in Unipolar Stochastic Logic .............109
  Yin Liu, Keshab K. Parhi (University of Minnesota, Twin Cities)

- DCC: Double Capacity Cache Architecture for Narrow-Width Values ..........................113
  Mohsen Imami, Shruti Patil, Tajana Rosing (University of California San Diego)

- Static Noise Margin based Yield Modelling of 6T SRAM for Area and Minimum Operating Voltage Improvement using Recovery Techniques ........................................117
  Nidhi Batra, Pawan Sehgal, Shashwat Kaushik, Mohammad S. Hashmi (IIT-Delhi),
  Sudesh Bhulla (ST Microelectronics), Anuj Grover (ST Microelectronics)

- Asynchronous High Speed Serial Links Analysis using Integrated Charge for Event Detection .................................................................121
  Aditya Dalakoti, Carrie Segal, Merritt Miller, Forrest Brewer (University of California Santa Barbara)

- Design and Comparative Evaluation of a Hybrid Cache Memory at Architectural Level .................................................................125
  Wei Wei (Northeastern University), Kazuteru Namba (Chiba University),
  Fabrizio Lombardi (Northeastern University)
• A Sampling Clock Skew Correction Technique for Time-Interleaved SAR ADCs .......... 129
  Daniel Prashanth, Hae-Seung Lee (Massachusetts Institute of Technology)

• Secure and Low-Overhead Circuit Obfuscation Technique with Multiplexers ............. 133
  Xueyan Wang, Xiaotao Jia, Qiang Zhou, Yici Cai (Tsinghua University), Jianlei Yang (University of Pittsburgh), Mingze Gao, Gang Qu (University of Maryland, College Park)

• Task-Resource Co-Allocation for Hotspot Minimization in Heterogeneous Many-Core NoCs ......................................................... 137
  Md Farhadur Reza, Dan Zhao, Hongyi Wu (University of Louisiana at Lafayette)

• Guiding Power/Quality Exploration for Communication-Intense Stream Processing ...... 141
  Hamed Tabkhi, Majid Sabghab, Gunar Schirner (Northeastern University)

Session 5: Low Power 1
Session Chair: Ioannis Savidis (Drexel University)

• Graphene-PLA (GPLA): A Compact and Ultra-Low Power Logic Array Architecture ...... 145
  Valerio Tenace, Andrea Calimera, Enrico Macii, Massimo Poncino (Politecnico di Torino)

• A Metastability Immune Timing Error Masking Flip-Flop for Dynamic Variation Tolerance ......................................................... 151
  Govinda Sannena, Bishnu Prasad Das (Indian Institute of Technology)

• Exploring Configurable Non-Volatile Memory-based Caches for Energy-Efficient Embedded Systems ........................................... 157
  Tosiron Adegbija (University of Arizona)

• Multiple Attempt Write Strategy for Low Energy STT-RAM ................................ 163
  Jaeyoung Park, Michael Orshansky (The University of Texas at Austin)

Special Session 1: IoT Security: Issues, Innovations and Interplays
Session Chair: Swarup Bhunia (University of Florida)

• Secret Sharing and Multi-User Authentication: From Visual Cryptography to RRAM Circuits .......................................................... 169
  Md Tanvir Arafin, Gang Qu (University of Maryland)

• Defense Systems and IoT: Security Issues in an Era of Distributed Command and Control ........................................................................ 175
  Doug Palmer, Saverio Fazzari (Booz Allen Hamilton), Scott Wartenberg (Wartenberg Consulting, LLC)

• Security Meets Nanoelectronics for Internet of Things Applications ...................... 181
  Garrett S. Rose (The University of Tennessee)

• Tracking Data Flow at Gate-Level through Structural Checking .............................. 185
  Thao Le, Jia Di (University of Arkansas), Mark Tehranipoor, Domenic Forte (University of Florida), Lei Wang (University of Connecticut)

Session 6: Test 2
Session Chair: Qiaoyan Yu (University of New Hampshire)

• Design of Error-Resilient Logic Gates with Reinforcement Using Implications .......... 191
  Xijing Han, Marco Donato, R. Iris Bahar, Alexander Zaslavsky, William Patterson (Brown University)

• Reducing Soft-Error Vulnerability of Caches using Data Compression ..................... 197
  Sparsh Mittal, Jeffrey S. Vetter (Oak Ridge National Laboratory)

• Workload-Aware Worst Path Analysis of Processor-Scale NBTI Degradation ............ 203
  Song Bian, Michihiro Shintani, Shumpei Morita, Hiromitsu Awano, Masayuki Hiromoto, Takashi Sato (Kyoto University)

• Enhancing Fault Emulation of Transient Faults by Separating Combinational and Sequential Fault Propagation ...................................... 209
  Ralph Nyberg, Johann Heyszl (Fraunhofer AISEC), Dietmar Heinz (Infineon Technologies AG), Georg Sigl (Fraunhofer AISEC & Technische Universität München)
Session 7: VLSI Circuits 2
Session Chair: Hai Li (University of Pittsburgh)

- **A Novel On-Chip Impedance Calibration Method for LPDDR4 Interface between DRAM and AP/SoC** ................................................................. 215
  Yongsuk Choi, Yong-Bin Kim (Northeastern University)

- **A General Sign Bit Error Correction Scheme for Approximate Adders** .................. 221
  Rui Zhou, Weikang Qian (University of Michigan-Shanghai Jiao Tong University Joint Institute)

- **RRAM Refresh Circuit: A Proposed Solution To Resolve The Soft-Error Failures For HfO2/Hf 1T1R RRAM Memory Cell** ........................................ 227
  Amr M.S. Tosson (University of Waterloo), Mohab Anis (American University at Cairo), Lan Wei (University of Waterloo)

- **Exploratory Power Noise Models of Standard Cell 14, 10, and 7 nm FinFET ICs** .......... 233
  Ravi Patel, Kan Xu, Eby G. Friedman (University of Rochester), Praveen Raghavan (IMEC Research)

- **8T1R: A Novel Low-power High-speed RRAM-based Non-volatile SRAM Design** ....... 239
  Amr M.S. Tosson, Adam Neale (University of Waterloo), Mohab Anis (American University at Cairo), Lan Wei (University of Waterloo)

Session 8: Emerging 1
Session Chair: Bo Yuan (City University of New York)

- **Polynomial Arithmetic Using Sequential Stochastic Logic** .................................. 245
  Naman Saraf, Kia Bazargan (University of Minnesota Twin Cities)

- **Ultra-Robust Null Convention Logic Circuit with Emerging Domain Wall Devices** .... 251
  Yu Bai, Bo Hu (University of Central Florida), Weidong Kuang (The University of Texas Rio Grande Valley), Mingjie Lin (University of Central Florida)

- **Inter-Tier Crosstalk Noise On Power Delivery Networks For 3-D ICs with Inductively-Coupled Interconnects** ......................................................... 257
  Ioannis A. Papistas, Vasilis F. Pavlidis (University of Manchester)

- **Delay Estimates for Graphene Nanoribbons: A Novel Measure of Fidelity and Experiments with Global Routing Trees** .......................................... 263
  Subrata Das (Jadavpur University), Soma Das (University of Calcutta), Adrijna Majumder, Parthasarathi Dasgupta (Indian Institute of Management Calcutta), Debesh Kumar Das (Jadavpur University)

Session 9: CAD 2
Session Chair: Miroslav Velev (Aries Design Automation)

- **VarDroid: Online Variability Emulation in Android/Linux Platforms** ....................... 269
  Pietro Mercati (University of California, San Diego), Francesco Patema (Intel Corporation), Andrea Bartolini (ETH Zurich/Univ. of Bologna), Mohsen Imani (University of California, San Diego), Luca Benini (ETH Zurich/Univ. of Bologna), Tajana Simunic Rosing (University of California, San Diego)

- **Neural Network-Based Prediction Algorithms for In-Door Multi-Source Energy Harvesting System for Non-Volatile Processors** ........................................ 275
  Ning Liu, Caiwen Ding, Yanzhi Wang (Syracuse university), Jingtong Hu (Oklahoma State University)

- **A Unified Model of Power Sources for the Simulation of Electrical Energy Systems** .... 281
  Sara Vinco, Yukai Chen, Enrico Macii, Massimo Poncino (Politecnico di Torino)

- **Hardware-Accelerated Software Library Drivers Generation for IP-Centric SoC Designs** ................................................................................................. 287
  Munish Jas, Uzair Sharif, Daniel Müller-Gritschneder, Ulf Schlichtmann (Technische Universität München)

- **Extracting Designs of Secure IPs Using FPGA CAD Tools** ..................................... 293
  Vincent Mirian, Paul Chow (University of Toronto)
Special Session 3: Emerging Technology Devices and Security
Session Chair: JV Rajendran (UT Dallas)

- **Security Primitive Design with Nanoscale Devices: A Case Study with Resistive RAM** ................................................................. 299
  Robert Karam (University of Florida), Rui Liu, Pai-Yu Chen, Shimeng Yu (Arizona State University), Swarup Bhunia (University of Florida)

- **Enhancing Hardware Security with Emerging Transistor Technologies** ............................... 305
  Yu Bi (University of Central Florida), X. Sharon Hu (University of Notre Dame), Yier Jin (University of Central Florida), Michael Niemier (University of Notre Dame), Kaveh Shamsi (University of Central Florida), Xunzhao Yin (University of Notre Dame)

- **The Applications of NVM Technology in Hardware Security** ..................................................... 311
  Chaofei Yang, Beiye Liu, Yandan Wang, Yiran Chen, Hai Li (University of Pittsburgh), Xian Zhang, Guangyu Sun (Peking University)

- **Survey of Emerging Technology Based Physical Unclonable Functions** .................................. 317
  Ilia A. Bautista Adames, Jayita Das, Sanjukta Bhanja (University of South Florida)

Session 10: VLSI Design 2
Session Chair: Brett Meyer (McGill University)

- **Trellis-search based Dynamic Multi-Path Connection Allocation for TDM-NoCs** ................. 323
  Yong Chen, Emil Matus, Gerhard Fettweis (Dresden University of Technology)

- **Prolonging Lifetime of Non-volatile Last Level Caches with Cluster Mapping** .................. 329
  Mortezasoltani, Mohammad Ebrahimi, Zainalabedin Navabi (University of Tehran)

- **A Low-Power Network-on-Chip Architecture for Tile-based Chip Multi-Processors** .......... 335
  Anastasios Psarras (Democritus University of Thrace), Junghee Lee (University of Texas at San Antonio), Pavlos Mattheakis (Mentor Graphics), Chrysostomos Nicopoulos (University of Cyprus), Giorgos Dimitrakopoulos (Democritus University of Thrace)

- **Dynamic Real-Time Scheduler for Large-Scale MPSoCs** ............................................................ 341
  Marcelo Ruaro, Fernando G. Moraes (PUCRS University)

Special Session 4: Emerging Frontiers in Hardware Security
Session Chairs: Ajay Joshi & (Boston University), Gang Qu (University of Maryland)

- **Leveraging 3D Technologies for Hardware Security: Opportunities and Challenges** ...... 347
  Peng Gu, Shuangchen Li, Dylan Stow, Russell Barnes, Liu Liu, Yuan Xie (University of California, Santa Barbara), Eren Kursun (Columbia University)

Poster Session 2
Session Chair: Hamed Tabkhi (Northeastern University)

- **FCM: Towards Fine-Grained GPU Power Management for Closed Source Mobile Games** ................................................................. 353
  Jiachen Song, Xi Li, Beliee Sun, Zhinan Cheng, Chao Wang, Xuehai Zhou (University of Science and Technology of China (USTC))

- **Quality of Service-Aware, Scalable Cache Tuning Algorithm in Consumer-Based Embedded Devices** ................................................................. 357
  Mohamad Hammam Alsafrijalani, Ann Gordon-Ross (University of Florida)

- **Temperature-Aware Dynamic Voltage Scaling for Near-Threshold Computing** ................. 361
  Saman Kiamehr, Mojtaba Ebrahimi, Mehdi Tahoori (Karlsruhe Institute of Technology (KIT))
- Leakage Power Minimization in Deep Sub-Micron Technology by Exploiting Positive Slacks of Dependent Paths ................................................................. 365
  Tulun Subhra Chakraborty, Santanu Kundu, Deepak Agrawal, Sanjay Tanaji Shinde, Jacob Mathews (Broadcom Limited), Rekha K. James (Cochin University of Science & Technology)

- An Enhanced Analytical Electrical Masking Model for Multiple Event Transients ........ 369
  Adam Watkins, Spyros Tragoudas (Southern Illinois University Carbondale)

- Capturing True Workload Dependency of BTI-induced Degradation in CPU Components ................................................................. 373
  Dimitrios Stamoulis (McGill University/imec vzw), Simone Corbetta (imec vzw/Katholieke Universiteit Leuven), Dimitrios Rodopoulos (National Technical University of Athens/Katholieke Universiteit Leuven), Pieter Weckx (imec vzw/Katholieke Universiteit Leuven), Peter Debacker (imec vzw), Brett H. Meyer (McGill University), Ben Kaczer, Praveen Raghavan (imec vzw), Dimitrios Soudris (National Technical University of Athens), Francky Catthoor (imec vzw/Katholieke Universiteit Leuven), Zeljko Zilic (McGill University)

- Performance Constraint-Aware Task Mapping to Optimize Lifetime Reliability of Manycore Systems ................................................................. 377
  Vijeta Rathore, Vivek Chaturvedi, Thambipillai Srikanthan (Nanyang Technological University (NTU))

- ASIC Implementation of An All-digital Self-adaptive PVT-A Variation-aware Clock Generation System ................................................................. 381
  Jordi Pérez-Puigdemont, Francesc Moll (Universitat Politècnica de Catalunya)

- Ultra-Low Energy Reconfigurable Spintronic Threshold Logic Gate .......................... 385
  Deliang Fan (University of Central Florida)

- Red-Shield: Shielding Read Disturbance for STT-RAM Based Register Files on GPUs ................................................................. 389
  Hang Zhang, Xuhao Chen, Nong Xiao, Fang Liu, Zhiguang Chen (National University of Defense Technology)

- Modeling and Study of Two-BDT-Nanostructure Based Sequential Logic Circuits ........ 393
  Poorna Marthi, Sheikh Rufsan Reza, Nazir Hossain, Jean-François Millihaier, Martin Margala (University of Massachusetts, Lowell), Ignacio Iñiguez-de-la-Torre, Javier Mateos, Tomás González (Universidad de Salamanca)

Session 11: Emerging 2
Session Chair: Jianwen Dai (Intel)

- Exploring Main Memory Design Based on Racetrack Memory Technology .................. 397
  Qingda Hu (Tsinghua University), Guangyu Sun (Peking University), Jiwue Shu (Tsinghua University), Chao Zhang (Peking University)

- An Offline Frequent Value Encoding for Energy-Efficient MLC/TLC Non-Volatile Memories ................................................................. 403
  Ali Alsuwaiyan, Kartik Mohanram (University of Pittsburgh)

- Low-Power Multi-Port Memory Architecture based on Spin Orbit Torque Magnetic Devices ................................................................. 409
  Rajendra Bishnoi, Fabian Oboril, Mehdi B. Tahoori (Karlsruhe Institute of Technology)

- Optimizing the Operating Voltage of Tunnel FET-Based SRAM Arrays Equipped with Read/Write Assist Circuitry .............................................. 415
  Hassan Afzali-Kusha, Alireza Shafraki, Massoud Pedram (University of Southern California)

Session 12: Low Power 2
Session Chair: Kyung Ki Kim (Daegu University), Bishnu Prasad Das (Indian Institute of Technology)

- Approximate Differential Encoding for Energy-Efficient Serial Communication ........ 421
  Daniele Jahier Pagliari, Enrico Macii, Massimo Poncino (Politecnico di Torino)

- Fast Thermal Simulation using SystemC-AMS .......................................................... 427
  Yukai Chen, Sara Vinco, Enrico Macii, Massimo Poncino (Politecnico di Torino)
• Learning-Based Near-Optimal Area-Power Trade-Offs in Hardware Design for Neural Signal Acquisition ................................................................. 433
  Cosimo Aprile (LIONS & LSM, EPFL), Luca Baldassarre, Vipul Gupta (LIONS, EPFL), Juhwan Yoo (Broadcom), Mahsa Shoaran (MICS, Caltech), Yusuf Leblebici, Volkan Cevher (LIONS, EPFL)

• Load Balanced On-Chip Power Delivery for Average Current Demand ........................................... 439
  Divya Pathak (Drexel University), Mohammad Hossein Hajkazemi, Mohammad Khavari Tavana, Houman Homayoun (George Mason University), Ioannis Savidis (Drexel University)

Author Index .................................................................................................................................................. 445