2016 IEEE Silicon Nanoelectronics Workshop (SNW 2016)

Honolulu, Hawaii, USA
12-13 June 2016
2016 IEEE Silicon Nanoelectronics Workshop

Hilton Hawaiian Village, Honolulu, HI USA

June 12-13, 2016

Technical Program

Opening Remarks
Sunday, June 12, 8:30 a.m.
Yee-Chia Yeo, TSMC

Session 1: Plenary
Sunday, June 12, 8:40 a.m.
Session Chair: Yee-Chia Yeo, TSMC

8:40 AM 1.1 (Plenary) Devices and Circuits at the End of Scaling, D. J. Frank, IBM 16

9:10 AM 1.2 (Plenary) Transport in Non-conventional FETs, J. Appenzeller, Purdue University 18

Session 2: 2D Materials and Devices
Session Chair: Shunri Oda, Tokyo Institute of Technology

9:40 AM 2.1 Enhancement of Inter-Band Tunneling Due to Low-Dimensionality of Lateral 2D Silicon Esaki Diodes, D. Moraru, H. N. Tan, L. T. Anh¹, M. Manoharan¹, T. Mizuno, R. Nuryadi², H. Mizuta¹,³, M. Tabe, Shizuoka University, ¹JAIST, ²Agency for Assessment and Application of Technology, ³Univ. of Southampton 20

9:55 AM 2.2 Thermal Limitations of Two-Dimensional Semi-Metallic WTe² Devices, R. Xu, M. Mleczko, S. Bohaichuk, Y. Nishi, E. Pop, Stanford University 22

10:10 AM 2.3 Black Phosphorus Transistors with Enhanced Hole Transport and Subthreshold Swing using Ultra-Thin HfO² High-k Gate Dielectric, Z.-P. Ling, X. Feng, H. Jiang², Z. He², X. Liu¹, K.-W. Ang, National University of Singapore, ¹Shenzen University, ²South University of Science and Technology of China 24

Coffee Break 10:25 a.m. – 10:45 a.m.
Session 3: Physics of Nanoscale Devices
Sunday, June 12, 10:45 a.m.
Session Chair: Eric Pop, Stanford University

10:45 AM  3.1 Dynamics of Electrically Driven Sub-nanosecond Switching in Vanadium Dioxide, M. Jerry, N. Shukla, H. Paik[1], D. G Schlom[1], S. Datta, University of Notre Dame, [1]Cornell University

11:00 AM  3.2 Coherent Control of Trapped-charge Induced Resonances in a Field-Effect Transistor, J. O. Tenorio-Pearl, E. D. Herbschleb, C. Creatore[1], A. Chin[1], S. Oda, Tokyo Institute of Technology, [1]University of Cambridge


11:45 AM  3.5 Energy Band Gap and Phonon Frequency in Semiconductors are Material Constants ?, S. Kabuyanagi, A. Toriumi, The University of Tokyo

Session 4: Nonvolatile Memory
Sunday, June 12, 1:30 p.m.
Session Chair: Pei-Wen Li, National Chiao Tung University


2:00 PM  4.2 Self-selection RRAM Cell with Sub-μA Switching Current and Robust Reliability Fabricated by High-K/Metal Gate CMOS Compatible Technology, P. Huang, S. Chen, Y. Zhao, B. Chen[1], B. Gao[2], L. Liu, X. Liu, J. Kang, Peking University, [1]University of Michigan, [2]Tsinghua University

2:15 PM  4.3 Multilevel Conductance Switching of a HfO2 RRAM Array Induced by Controlled Filament for Neuromorphic Applications, J. Woo, J. Song, K. Moon, S. Lee, J. Park, H. Hwang, Pohang University of Science and Technology (POSTECH)

2:30 PM  4.4 Vertical versus Lateral Tunneling FET Non-Volatile Memory Cell, A. Biswas, S. Tomar, A. M. Ionescu, EPFL
3:00 PM


Coffee Break 3:15 p.m. – 3:35 p.m.

Session 5: New Memory Architecture for Neuromorphic Applications
Sunday, June 3:35 p.m.
Session Chair: Heike Riel, IBM Research Zurich

3:35 PM


4:05 PM

5.2 (Invited) Computing with Coupled Dynamical Systems, S. Datta, N. Shukla, A. Parihar, A. Raychowdhury, University of Notre Dame, 1Georgia Institute of Technology

4:35 PM

5.3 A Hardware Neural Network for Handwritten Digits Recognition Using Binary RRAM as Synaptic Weight Element, W. Wang, Y. Li, M. Wang, L. Wang, Q. Liu, W. Banerjee, L. Li, M. Liu, Institute of MicroElectronics of the Chinese Academy of Sciences (IMECAS), also with 1University of Chinese Academy of Sciences (UCAS)

Poster Session 1
Sunday, June 12, 4:55 p.m. – 7:00 p.m.
4:55 p.m. Poster Introductions (1 minute each)
Session Co-Chairs: Steve Chung, National Chiao Tung University, and Adrian Ionescu, EPFL


P1-2 Synthesis of Wafer-Scale WSe₂ by WOx Selenization on SiO₂ / Si Substrates, Y. C. Chu, C.- A. Jong, Y. T. Ho, M. Zhang, P.-Y. Chien, H. R. Hsu, H.-Y. Chen, Y.-Y. Tu, K. P. Pande, J. Woo, E. Y. Chang, National Chiao Tung University, 1National Nano Device Laboratories, 2University of California, Los Angeles, 3Industrial Technology Research Institute

P1-3 High-mobility 2D layered Semiconducting Transistors Based on Large-area and Highly Crystalline CVD-grown MoSe₂ for Flexible Electronics, S. Hong, S. M. Kim, W. G. Song, Y. Hong, S. Kim, Kyung Hee University, 1Korea Institute of Science and Technology
P1-4 Reliable Doping Technique for WSe2 by W:Ta Co-Sputtering Process, P.-Y. Chien, M. Zhang, S.-C. Huang1, M.-H. Lee1, H. R. Hsu2, Y. T. Ho3, Y. C. Chu3, C.-A. Jong4, J. Woo, University of California, Los Angeles, 1National Taiwan Normal University, 2ITRI, 3National Chiao Tung University, 4National Nano Device Laboratories

P1-5 Atomically Flat Metal-Insulator-Metal Capacitors with Enhanced Linearity, C.-H. Huang, S.-T. Fan, P.-S. Chen, R. Sankar, F.-C. Chou, C. W. Liu1,2, National Taiwan University, 1Institute of Atomic and Molecular Sciences, 2Academia Sinica

P1-6 Quantifying the Impact of Thickness and Drain Bias on Black Phosphorus Field Effect Transistor Performance, N. Haratipour, S. J. Koester, University of Minnesota-Twin Cities

P1-7 Fabrication and RTN Characteristics of Gate-All-Around Poly-Si Junctionless Nanowire Transistors, C.-C. Yang, Y.-C. Chen, H.-C. Lin, R. D. Chang1, P.-W. Li, T.-Y. Huang, National Chiao Tung University, 1Chang Gung University

P1-8 Short-Channel ZnON Thin-Film Transistors with Film Profile Engineering, H. -C. Lin, C. –I. Kuan, P.-W. Li, T.-Y. Huang, National Chiao Tung University

P1-9 Antenna-Coupled Single-Metal Nanothermocouples for THz Wave Detection, G. Szakmany, A. Orlov, G. Bernstein, W. Porod, University of Notre Dame


P1-12 Stable Unipolar and Bipolar Resistive Transitions of Sputter-Deposited SiO2 Films, R. Yamaguchi, T. Akano, S. Sato, Y. Omura, Kansai University


P1-14 Analog Memory Characteristics of 1T1R MoOx Resistive Random Access Memory, M. Jo, R. Katsumura, A. Tsurumaki-Fukuchi, M. Arita, Y. Takahashi, H. Ando1, T. Morie1, Hokkaido University, 1Kyushu Institute of Technology

P1-16 Ultrafast Switching in Ta$_2$O$_5$-based Resistive Memories, V. Havel, K. Fleck, B. Rösgen$^1$, V. Rana$^1$, S. Menzel$^1$, U. Böttger, R. Waser$^1$, RWTH Aachen, $^1$Forschungszentrum Jülich

P1-17 Improved Endurance of RRAM by Optimizing Reset Bias Scheme in 1T1R Configuration to Suppress Reset Breakdown, C. Sung, J. Song, S. Lee, H. Hwang, Pohang University of Science and Technology (POSTECH)

P1-18 Reliability Study of Carbon Nanotube Memory after Various Cycling Conditions, I. Takashi, T. O. Iwasaki, S. Ning$^1$, D. Viviani$^1$, M. Manning$^1$, H. Huang$^1$, T. Rueckes$^1$, K. Takeuchi, Chuo University, $^1$Nantero Inc.

P1-19 Optimal Combinations of SCM Characteristics and Non-volatile Cache Algorithms for High-Performance SCM/NAND Flash Hybrid SSD, T. Yamada, C. Matsui, T. Ken, Chuo University


P1-21 Storage Class Memory Based SSD Performance in Consideration of Error Correction Capabilities and Write/Read Latencies, H. Takishita, T. Onagi, K. Takeuchi, Chuo University


P1-25 Formation of GeSn-On-Insulator (GeSnOI) Substrate using Direct Wafer Bonding, D. Lei, K. H. Lee$^1$, S. Bao$^{1,2}$, W. Wang, B. Wang$^1$, X. Gong, C. S. Tan$^2$, Y. C. Yeo, National University of Singapore, $^1$Singapore MIT Alliance for Researchand Technology (SMART), $^2$Nanyang Technological University
P1-27 Spin Accumulation in a Si Channel using High-Quality CoFe/MgO/Si Spin Injectors, T. Akushichi, D. Kitagata, Y. Takamura, Y. Shuto, S. Sugahara, Tokyo Institute of technology

P1-28 Improved Electrical and Reliability Characteristics in Ge p-MOSFETs with In-situ Plasma Treatments and Capping Hf/Zr on Interfacial Layers, Y.-L. Li, K.-S. Chang-Liao, S.-H. Yi, National Tsing Hua University

P1-29 Re-examination the Effects of Selenium Segregation on the Schottky Barrier Height Reduction of the NiGe/Ge Contact, Y.-J. Chen, H.-J. Chou, C.-J Li, B.-Y. Tsui, National Chiao Tung University, 1Advanced Ion Beam Technology, Inc.


P1-33 Electrical characterization of back-gated and top-gated germanium-core/silicon-shell nanowire field-effect transistors, M. Simanullang, G.B. M. Wisna, W. Cao, K. Usami, K. Banerjee, S. Oda, Tokyo Institute of Technology, 1Bandung Institute of Technology, 2University of California, Santa Barbara

P1-34 An Area Efficient Gate-All-Around Ring MOSFET, Y. –C. Huang, M. –H. Chiang, S. -J. Wang, National Cheng Kung University,
Session 6: Novel Group IV Electronics and Photonics  
Monday, June 13, 8:30 a.m.  
Session Chair: Toshihiro Hiramoto, University of Tokyo

8:30 AM  

9:00 AM  

Session 7: High Mobility and III-V Devices  
Monday, June 13, 9:15 a.m. – 10:30 a.m.  
Session Chair: Lars-Erick Wernersson, University of Lund

9:15 AM  
7.1 In0.30Ga0.70As QW MOSFETs with Peak Mobility exceeding 3000 cm²/V•s Fabricated on Si Substrates, S. Yadav, Annie, D. Kohen, X. S. Nguyen, K. H. Lee, X. Gong, D. Antoniadis, E. Fitzgerald, Y. C. Yeo, National University of Singapore, Singapore-MIT Alliance for Research & Technology, Electrical Engineering, Massachusetts Institute of Technology, Materials Science, Massachusetts Institute of Technology

9:30 AM  
7.2 High-mobility GeSn p-MOSFETs on Transparent Substrate Utilizing Nucleation-controlled Liquid-phase Crystallization, H. Oka, T. Amamoto, T. Hosoi, T. Shimura, H. Watanabe, Osaka University

9:45 AM  

10:00 AM  
7.4 Strained Ge0.91Sn0.09 Quantum Well p-MOSFETs, Y.-S. Huang, C.-H. Huang, F.-L. Lu, D.-Z. Chang, C.-Y. Lin, I.-H. Wong, S. R. Jan, H.-S. Lan, C. W. Liu, Y.-C. Huang, H. Chung, C.-P. Chang, S. S. Chu, S. Kuppurao, National Taiwan University, also with National Nano Device Laboratories, Applied Materials Inc.

10:15 AM  
7.5 (Invited) Neutral Beam Technology: Defect-free Nanofabrication for Novel Nano-materials and Nano-devices, S. Samukawa, Tohoku University

Coffee Break 10:45 a.m. – 11:05 a.m.
Session 8: Advanced CMOS and New Device Concepts
Monday, June 13, 11:05 a.m.
Session Chair: Wolfgang Porod, University of Notre Dame

11:05 AM 8.1 Stacked Nanowires FETs: Mechanical Robustness Evaluation for sub-7nm Nodes, L. Gaben, A. Arnaud, M. Barlas¹, M. P. Samson, C. Arvet, C. Vizioz¹, J.-M. Hartmann¹, S. Barraud¹, S. Monfray, F. Boeuf, T. Skotnicki, F. Balestra², M. Vinet¹, STMicroelectronics, ¹CEA-LETI, ²IMEP-LAHC

11:20 AM 8.2 Increased Drain-Induced Variability and Within-Device Variability in Extremely Narrow Silicon Nanowire MOSFETs with Width down to 2nm, T. Mizutani, K. Takeuchi, R. Suzuki, T. Saraya, M. Kobayashi, T. Hiramoto, The University of Tokyo

11:35 AM 8.3 Considerations on Fermi-Depinning, Dipoles and Oxide Tunneling for Oxygen-based Dielectric Insertions in Advanced CMOS Contacts, J. Borrel²,³, L. Hutin¹, H. Grampeix¹, E. Nolot¹, E. Ghegin¹, P. Rodriguez¹, C. Tabone¹, F. Allain¹, J.-P. Barnes¹, Y. Morand, F. Nemouchi¹, M. Gregoire, E. Dubois², M. Vinet¹, STMicroelectronics, ¹CEA, LETI, ²IEMN, CNRS

11:50 AM 8.4 Charge Pumping EDMR Towards Charge/spin Manipulation in Silicon at Room Temperature, M. Hori, R. Narimatsu¹, Y. Ono¹, Shizuoka University, ¹University of Toyama

12:05 PM 8.5 Atomic-Precision Architectures for the High-Fidelity Spin Read-out of Phosphorus Donors in Silicon, B. Weber¹, T. F. Watson¹, M. Y. Simmons, The University of New South Wales, also with ¹Monash University

Session 9: Low Power and Steep-slope Devices
Monday, June 13, 1:30 p.m.
Session Chair: Maud Vinet, CEA-LETI, Grenoble

1:30 PM 9.1 (Invited) Ultra-low Power and Ultra-low Voltage Devices and Circuits for IoT Applications, T. Hiramoto, K. Takeuchi, T. Mizutani, A. Ueda, T. Saraya, M. Kobayashi, Y. Yamamoto¹, H. Makiyama¹, T. Yamashita¹, H. Od¹, S. Kamohara¹, N. Sugii¹, Y. Yamaguchi¹, The University of Tokyo, ¹Leap

2:00 PM 9.2 Confirmation of SS= 35μV/dec over 3 Decades of Drain Current and Hole Accumulation Effect on PN-Body Tied SOI Super Steep SS FET’s, T. Horii, J. Ida, T. Yoshida, M. Okihara¹, Y. Arai², Kanazawa Institute of Technology, ¹LAPIS Semiconductor Co., Ltd., ²High Energy Accelerator Research Org., KEK

2:15 PM 9.3 Negative Capacitance as a Performance Booster for Tunnel FET, M. Kobayashi, K. Jang, N. Ueyama, T. Hiramoto, The University of Tokyo
2:30 PM  9.4 Investigation of Doping in InAs/GaSb Hetero-junctions for Tunnel-FETs, D. Cutaia, H. Schmid, M. Borg1, K. E. Moselund, N. Bologna2, A. Olziensky, A. Ionescu3, H. Riel, IBM Research - Zurich, also with 1Lund University, 2Empa, Swiss Federal Laboratories for Materials Science and Technology, 3École Polytechnique Federal de Lausanne, EPFL

2:45 PM  9.5 InAs/GaSb Vertical Nanowire TFETs on Si for Digital and Analogue Applications, E. Memišević, J. Svensson, E. Lind, L.-E. Wernersson, Lund University

Coffee Break 3:00 p.m. – 3:20 p.m.

Poster Session 2
Monday, June 13, 3:25 p.m. – 5:30 p.m.
3:25 p.m. Poster Introductions (1 minute each)
Session Co-Chairs: Adrian Ionescu, EPFL, and Steve Chung, National Chiao Tung University

P2-1 Device Optimization on Gate Oxide and Spacer Dielectric Permittivity for well-tempered Nanoscale MOSFET", E. Jang, S. Shin, J. W. Jung, Y. Jung, K. R. Kim, Ulsan National Institute of Science and Technology


P2-3 High Quality Ge-OI, III-V-OI on 200 mm Si Substrate, K. H. Lee, Y. Lin1, S. Bao1, L. Zhang, K. Lee, J. Michel2, E. Fitzgerald2, C. S. Tan, Singapore-MIT Alliance for Research & Technology, 1Nanyang Technological University, 2Massachusetts Institute of Technology

P2-5 Development and Electrical Performance of Low Temperature Cu-Sn/In Bonding for 3D Flexible Substrate Integration, Y.-C. Hu, K.-N. Chen, National Chiao Tung University

P2-6 Nonvolatile Power-gating Architecture for SRAM using SOTB Technology, Y. Shuto, S. Yamamoto, S. Sugahara, Tokyo Institute of Technology

P2-7 PTM-based V1-Variability Analysis and Compensation of a Nanoscaled Comparator Circuit based on FinFETs and Resistive Switches, A. Heittmann, RT. Noll, WTH Aachen University

P2-8 Demonstration of Standrad Ternary Inverter Based on CMOS Technology, S. Shin, E. Jang, J. W. Jeong, K. R. Kim., Ulsan National Institute of Science and Technology, Ulsan National Institute of Science and Technology (UNIST)

P2-10 Capacitance Matching Effects in Negative Capacitance Field Effect Transistor, J. Jo, A. I. Khan¹, K. Cho, S. Oh, S. Salahuddin¹, C. Shin, University of Seoul, ¹University of California

P2-11 On Gate Stack Scalability of Double-Gate Negative-Capacitance FET with Ferroelectric HfO₂ for Energy-Efficient Sub-0.2V Operation, K. Jang, T. Saraya, M. Kobayashi, T. Hiramoto, The University of Tokyo

P2-12 Evaluation of the Origin of Excited States Appeared in Small Si Single-electron Transistors, T. Uchida, M. Jo, H. Satoh, A. Tsurumaki-Fukuchi, M. Arita, A. Fujiwara¹, Y. Takahashi, Hokkaido University, ¹NTT Corporation


P2-14 Cryogenic Operation of SOI Electron Pumps and Ring Oscillators, P. Clapera, X. Jehl, L. Hutin¹, S. Barraud¹, A. Valentian¹, S. De Franceschi, M. Sanquer, M. Viner¹, CEA, INAC-PHELIQS, ¹CEA-LETI


P2-16 A Possible Threshold Voltage Definition of Lateral Tunnel FET, Y. Mori, S. Sato, Y. Omura, A. Mallik², Kansai University, ²University of Calcutta

P2-17 3D-TCAD Simulation Study of the Contact All Around T-FinFET Structure for 10nm Metal-Oxide-Semiconductor Field-Effect Transistor, C. H. Chou, C.-C. Hsu, W.-K. Yeh¹, S. S. Chung, C.-H. Chien, National Chiao Tung University, ¹National Nano Device Laboratories

P2-18 Theoretical Analysis of High-field Hole Transport in Germanium and Silicon Nanowires, H. Tanaka, J. Suda, T. Kimoto, Kyoto University

P2-19 Atomistic Simulations of Hetero-junction Tunneling Field-Effect Transistors with Layered Black Phosphorus, F. Liu, J. Wang, H. Guo¹, The University of Hong Kong, ¹McGill University

P2-20 Evaluation the Degradation in nMOSFETs with HfO₂ Gate Dielectric and Interfacial Layer by 3D Kinetic Monte-Carlo Method, Y. Li, Z. Lun, Y. Wang, P. Huang, H. Jiang, X. Zhang, G. Du, X. Liu, Peking University

P2-21 Advanced Simulation of Resistance Switching in Si-Rich Silica RRAM Devices, T. Sadi, L. Wang, A. Asenov, University of Glasgow
200 P2-23 Robust Design of Electric-field-assisted Nonlocal Si-MOS Spin-devices, D. Kitagata, T. Akushichi, Y. Takamura, Y. Shuto, S. Sugahara, Tokyo Institute of Technology


P2-25 Performance Evaluation of Nanoscale FETs Based on Full-Band Complex Bandstructure and Real Space Poisson Solver, X. Zhang, Y.-C. Yeo, G. Liang, National University of Singapore


Additional Papers:

Activation of High Concentrations of Phosphorus in Germanium by Two-steps Microwave Annealing, Wen-Hsi Lee, Tzu-Lang Shih, Chia-Wei Lin, Yi-Chen Chung

Comparison of ZnO and Ti Doped ZnO Sensing Membrane in Bio-Sensor Applications Detector based on Field-Effect Transistor, Chyuan Haur Kao, Che Wei Chang, Chan-Yu Lin, Yen Lin Su, Chun Fu Lin, Chia Lun Chang, Chia Shao Liu

Improved Electrical and Reliability Characteristics in Ge p-MOSFETs with In-Situ Plasma Treatments and Capping Hf/Zr on Interfacial Layers, Yan-Lin Li, Kuei-Shu Chang-Liao, Shih-Han Yi

Investigation of Novel Vertical Super-Thin Body Silicon MOSFET Performance Advantages, Rimma Pirogova, Jeffrey Wolf, Viktor Koldiaev