
Austin, Texas, USA
7-10 November 2016
Proceedings of the 2016 International Conference on Computer-Aided Design (ICCAD)  
November 7 – 10, 2016  
Doubletree Hotel  
Austin, TX

1A.1 - Scope - Quality Retaining Display Rendering Workload Scaling based on User-Smartphone Distance  1  
Kent Nixon, Xiang Chen, Yiran Chen

1A.2 - NVsim-CAM: A Circuit-Level Simulator for Emerging Nonvolatile Memory based Content-Addressable Memory  7  
Shuangchen Li, Liu Liu, Peng Gu, Cong Xu, Yuan Xie

1A.3 - Design Technology for Fault-Free and Maximally-Parallel Wavelength-Routed Optical Networks-on-Chip  14  
Andrea Peano, Luca Ramini, Marco Gavanelli, Maddalena Nonato, Davide Bertozzi

1B.1 - Fast Generation of Lexicographic Satisfiable Assignments: Enabling Canonicity in SAT-Based Applications  22  
Ana Petkovska, Alan Mishchenko, Mathias Soeken, Giovanni De Micheli, Robert Brayton, Paolo Ienne

1B.2 - Analytic Approaches to the Collapse Operation and Equivalence Verification of Threshold Logic Circuits  30  
Nian-Ze Lee, Hao-Yuan Kuo, Yi-Hsiang Lai, Jie-Hong Roland Jiang

1B.3 - A Flash-based Digital Circuit Design Flow  38  
Monther Abusultan, Sunil P. Khatri

1C.1 - MrDP: Multiple-row Detailed Placement of Heterogeneous-sized Cells for Advanced Nodes  44  
Yibo Lin, Bei Yu, Xiaqing Xu, Jhih-Rong Gao, Natarajan Viswanathan, Wen-Hao Liu, Zhuo Li, David Z. Pan, Charles J. Alpert

1C.2 - OWARU: Free Space-Aware Timing-Driven Incremental Placement  52  
Jinwook Jung, Gi-Joon Nam, Lakshmi Reddy, Iris Hui-Ru Jiang, Youngsoo Shin

1C.3 - Detailed Placement for Modern FPGAs using 2D Dynamic Programming  60  
Shounak Dhar, Saurabh Adya, Love Singhal, Mahesh Iyer, David Z. Pan

1D.1 - Security and Privacy Threats to On-Chip Non-Volatile Memories and Countermeasures  68  
Swaroop Ghosh, Md. Nasim Imtiaz Khan, Asmit De, Jae-won Jang

1D.2 - Security Engineering of Nanostructures and Nanomaterials  74  
Davood Shahrjerdi, Bayan Nasri, Darren Armstrong, Abdullah S. Alharbi, Ramesh Karri

2A.1 - Caffeine: Towards Uniformed Representation and Acceleration for Deep Convolutional Neural Networks  79  
Chen Zhang, Zhenman Fang, Peipei Zhou, Peichen Pan, Jason Cong
2A.2 - Re-architecting the On-chip memory Sub-system of Machine-Learning Accelerator for Embedded Devices  87
Ying Wang, Huawei Li, Xiaowei Li

2A.3 - A Data Locality-aware Design Framework for Reconfigurable Sparse Matrix-Vector Multiplication Kernel  93
Sicheng Li, Yandan Wang, Wujie Wen, Yu Wang, Yiran Chen, Hai (Helen) Li

2A.4 - Compact Oscillation Neuron Exploiting Metal-Insulator-Transition for Neuromorphic Computing  99
Pai-Yu Chen, Jae-sun Seo, Yu Cao, Shimeng Yu

2B.1 - A New Tightly-Coupled Transient Electro-Thermal Simulation Method for Power Electronics  105
Quan Chen, Wim Schoenmaker

2B.2 - A Tensor-Based Volterra Series Black-Box Nonlinear System Identification And Simulation Framework  112
Kim Batselier, Zhongming Chen, Haotian Liu, Ngai Wong

2B.3 - Efficient Statistical Analysis for Correlated Rare Failure Events via Asymptotic Probability Approximation  119
Handi Yu, Jun Tao, Changhai Liao, Yangfeng Su, Dian Zhou, Xuan Zeng, Xin Li

2B.4 - Duplex: Simultaneous Parameter-Performance Exploration for Optimizing Analog Circuits  127
Seyed Nematollah Ahmadyan, Shobha Vasudevan

2C.1 - Improved Flop Tray-Based Design Implementation for Power Reduction  135
Andrew B. Kahng, Jiajia Li, Lutong Wang

2C.2 - RC-Aware Global Routing  143
Rudolf Scheifele

2C.3 - Scalable, High-Quality SAT-Based Multi-Layer Escape Routing  151
Sam Bayless, Holger H. Hoos, Alan J. Hu

2C.4 - Redistribution Layer Routing for Integrated Fan-Out Wafer-Level Chip-Scale Packages  159
Bo-Qiao Lin, Ting-Chou Lin, Yao-Wen Chang

2D.1 - The Architecture Value Engine: Measuring and Delivering Sustainable SoC Improvement  167
Juan-Antonio Carballo, Andrew B. Kahng

2D.2 - Circuit Valorization in the IC Design Ecosystem  172
Jose Pineda de Gyvez, Hamed Fatemi, Maarten Vertregt
2D.3 - Interconnect-aware Device Targeting from PPA Perspective  
Mustafa Badaroglu, Jeff Xu

2D.4 - Measuring Progress and Value of IC Implementation Technology  
Andrew B. Kahng, Hyein Lee, Jiajia Li

3A.1 - Provably Secure Camouflaging Strategy for IC Protection  
Meng Li, Kaveh Shamsi, Travis Meade, Zheng Zhao, Bei Yu, Yier Jin, David Z. Pan

3A.2 - CamoPerturb: Secure IC Camouflaging for Minterm Protection  
Muhammad Yasin, Bodhisatwa Mazumdar, Ozgur Sinanoglu, Jeyovijayan Rajendran

3A.3 - Chip Editor: Leveraging Circuit Edit for Logic Obfuscation and Trusted Fabrication  
Bicky Shakya, Navid Asadizanjani, Domenic Forte, Mark Tehranipoor

3B.1 - Arbitrary Streaming Permutations with Minimum Memory and Latency  
Thaddeus Koehn, Peter Athanas

3B.2 - Multi-bank Memory Optimization for Parallel Data Access in Multiple Data Arrays  
Shouyi Yin, Zhichong Xie, Chenyue Meng, Leibo Liu, Shaojun Wei

3B.3 - Allocation of Multi-bit Flip-flops in Logic Synthesis for Power Optimization  
Dongyoun Yi, Taewhan Kim

3C.1 - Model-based Design of Resource-efficient Automotive Control Software  
Wanli Chang, Debayan Roy, Licong Zhang, Samarjit Chakraborty

3C.2 - Testing Automotive Embedded Systems under X-in-the-Loop Setups  
Ghizlane Tibba, Christoph Malz, Christoph Stoermer, Natarajan Nagarajan, Licong Zhang, Samarjit Chakraborty

3C.3 - Efficient Statistical Validation of Machine Learning Systems for Autonomous Driving  
Weijing Shi, Mohamed Baker Alawieh, Xin Li, Huafeng Yu, Nikos Areshiga, Nobuyuki Tomatsu

3C.4 - CONVINCE: A Cross-Layer Modeling, Exploration and Validation Framework for Next-Generation Connected Vehicles  
Bowen Zheng, Chung-Wei Lin, Huafeng Yu, Hengyi Liang, Qi Zhu

3D.1 - Overview of the 2016 CAD Contest at ICCAD  
Shih-Hsu Huang, Rung-Bin Lin, Myung-Chul Kim, Shigetoshi Nakatake

3D.2 - ICCAD-2016 CAD Contest in Large-scale Identical Fault Search  
Tien-Chun (Tangent) Wei, Kuo-Ching (Luke) Lin
4C.3 - Exact Diagnosis using Boolean Satisfiability  366
Heinz Rienner, Goerschwin Fey

4C.4 - Efficient and Accurate Analysis of Single Event Transients Propagation Using SMT-Based Techniques  374
Ghaith Bany Hamad, Ghaith Kazma, Otmane ait Mohamed, Yvon Savaria

4D.1 - Power Delivery in 3D Packages: Current Crowding Effects, Dynamic IR Drop and Compensation Network using Sensors  381
Sukeshwar Kannan, Mehdi Sadi, Luke England

4D.2 - Cost Analysis and Cost-Driven IP Reuse Methodology for SoC design Based on 2.5D/3D Integration  387
Dylan Stow, Itir Akgun, Peng Gu, Russell Barnes, Yuan Xie

4D.3 - Energy-Efficient and Reliable 3D Network-on-Chip (NoC): Architectures and Optimization Algorithms  393
Sourav Das, Janardhan Rao Doppa, Partha Pratim Pande, Krishnendu Chakrabarty

4D.4 - The Hype, Myths, and Realities of Testing 3D Integrated Circuits  399
Ran Wang, Sergej Deutsch, Mukesh Agrawal, Krishnendu Chakrabarty

Leonidas Kosmidis, Roberto Vargas, David Morales, Eduardo Quiñones, Jaume Abella, Francisco J. Cazorla

5A.2 - Splitting Functions in Code Management on Scratchpad Memories  415
Youngbin Kim, Jian Cai, Yooseong Kim, Kyoungwoo Lee, Aviral Shrivastava

5A.3 - Adaptive Performance Prediction for Integrated GPUs  423
Ujjwal Gupta, Joseph Campbell, Umit Y. Ogras, Raid Ayoub, Michael Kishinevsky, Francesco Paterna, Suat Gumussoy

5B.1 - Energy-efficient Fault Tolerance Approach for Internet of Things Applications  431
Teng Xu, Miodrag Potkonjak

5B.2 - Critical Path Isolation for Time-to-Failure Extension and Lower Voltage Operation  439
Yutaka Masuda, Masanori Hashimoto, Takao Onoye

5B.3 - Control Synthesis and Delay Sensor Deployment for Efficient ASV Designs  447
Chaofan Li, Sachin Sapatnekar, Jiang Hu

5C.1 - Performance Driven Routing for Modern FPGAs  454
Parivallal Kannan, Satish Sivaswamy
5C.2 - UTPlaceF: A Routability-Driven FPGA Placer with Physical and Congestion Aware Packing 460
Wuxi Li, Shounak Dhar, David Z. Pan

5C.3 - RippleFPGA: A Routability-Driven Placement for Large-Scale Heterogeneous FPGAs 467
Chak-Wa Pui, Gengjie Chen, Wing-Kai Chow, Ka-Chun Lam, Jian Kuang, Peishan Tu, Hang Zhang, Evangeline F.Y. Young, Bei Yu

5C.4 - GPlace - A Congestion-aware Placement tool for UltraScale FPGAs 475
Ryan Pattison, Ziad Abuowaimer, Shawki Areibi, Gary Grewal, Anthony Vannelli

5D.1 - Resiliency in Dynamically Power Managed Designs 482
Liangzhen Lai, Vikas Chandra, Rob Aitken

5D.2 - Dynamic Reliability Management for Near-Threshold Dark Silicon Processors 488
Taeyoung Kim, Zeyu Sun, Chase Cook, Jagadeesh Gaddipati, Hai Wang, Haibao Chen, Sheldon Tan

5D.3 - A Cross-Layer Approach for Resiliency and Energy Efficiency in Near Threshold Computing 495
Mohammad Saber Golanbari, Anteneh Gebregiorgis, Fabian Oboril, Saman Kiamehr, Mehdi Tahoori

6A.1 - Design Space Exploration of Drone Infrastructure for Large-Scale Delivery Services 503
Sangyoung Park, Licong Zhang, Samarjit Chakraborty

6A.2 - Multi-Objective Design Optimization for Flexible Hybrid Electronics 510
Ganapati Bhat, Ujjwal Gupta, Nicholas Tran, Jaehyun Park, Sule Ozev, Umit Y. Ogras

6A.3 - KCAD: Kinetic Cyber Attack Detection Method for Cyber-Physical Additive Manufacturing Systems 518
Sujit Rokka Chhetri, Arquimedes Canedo, Mohammad Al Faruque

6A.4 - Autonomous Sensor-Context Learning in Dynamic Human-Centered Internet-of-Things Environments 526
Seyed Ali Rokni, Hassan Ghasemzadeh

6B.1 - Formulating Customized Specifications for Resource Allocation Problem of Distributed Embedded Systems 532
Xinhai Zhang, Lei Feng, Martin Törngren, De-Jiu Chen

6B.2 - A Polyhedral Model-based Framework for Dataflow Implementation on FPGA devices of Iterative Stencil Loops 540
Giuseppe Natale, Giulio Stramondo, Pietro Bressana, Riccardo Cattaneo, Donatella Sciuto, Marco D. Santambrogio

6B.3 - Efficient Memory Compression in Deep Neural Networks Using Coarse-Grain Sparsification for Speech Applications 548
Deepak Kadetotad, Sairam Arunachalam, Chaitali Chakrabarti, Jae-sun Seo
6B.4 - Parallel Code-Specific CPU Simulation with Dynamic Phase Convergence Modeling for HW/SW Co-Design 556
Warren Kemmerer, Wei Zuo, Deming Chen

6C.1 - Architectural-Space Exploration of Approximate Multipliers 564
Semeen Rehman, Walaa El-Harouni, Muhammad Shafique, Akash Kumar, Jörg Henkel

6C.2 - Design of Power-Efficient Approximate Multipliers for Approximate Artificial Neural Network 572
Vojtech Mrazek, Syed Shakib Sarwar, Lukas Sekanina, Zdenek Vasicek, Kaushik Roy

6C.3 - Automated Error Prediction for Approximate Sequential Circuits 579
Amrut Kapare, Hari Cherupalli, John Sartori

6C.4 - Approximation-aware Rewriting of AIGs for Error Tolerant Applications 587
Arun Chandrasekharan, Mathias Soeken, Daniel Grosse, Rolf Drechsler

6D.2 - Properties First? A New Design Methodology for Hardware, and its Perspectives in Safety Analysis 595
Joakim Urdahl, Shrinidhi Udupi, Tobias Ludwig, Dominik Stoffel, Wolfgang Kunz

6D.3 - Where Formal Verification Can Help in Functional Safety Analysis 603
Alessandro Bernardini, Wolfgang Ecker, Ulf Schlichtmann

6D.4 - Formal Approaches to Design of Active Cell Balancing Architectures in Battery Management Systems 611
Sebastian Steinhorst, Martin Lukasiewycz

7A.1 - How Much Cost Reduction Justifies the Adoption of Monolithic 3D ICs at 7nm Node? 617
Bon Woong Ku, Peter Debacker, Dragomir Milojevic, Praveen Raghavan, Sung Kyu Lim

7A.2 - A Novel Unified Dummy Fill Insertion Framework with SQP-Based Optimization Method 624
Yudong Tao, Changhao Yan, Yibo Lin, Shengguo Wang, David Z. Pan, Xuan Zeng

7A.3 - Efficient Yield Estimation through Generalized Importance Sampling with Application to NBL-Assisted SRAM bitcells 632
Lorenzo Ciampilini, Xavier Jonsson, Cyril Descloes, Jean-Christophe Lafont, Faress Tissafi Drissi, Jean-Paul Morin, David Turgis, Joseph Nguyen

7B.1 - Are Proximity Attacks a Threat to the Security of Split Manufacturing of Integrated Circuits? 640
Jonathon C. Magaña, Daohang Shi, Azadeh Davoodi

7B.2 - Making Split-Fabrication More Secure 647
Ping-Lin Yang, Malgorzata Marek-Sadowska
7B.3 - A Machine Learning Approach to Fab-of-Origin Attestation 655
Ali Ahmadi, Mohammad-Mahdi Bidmeshki, Amit Nahar, Bob Orr, Michael Pas, Yiorgos Makris

7C.1 - OpenRAM: An Open-Source Memory Compiler 661
Matthew Guthaus, James Stine, Samira Ataei, Brian Chen, Bin Wu, Mehedi Sarwar

8A.1 - A Hardware-based Technique for Efficient Implicit Information Flow Tracking 667
Jangseop Shin, Hongce Zhang, Jinyong Lee, Ingoo Heo, Yu-Yuan Chen, Ruby Lee, Yunheung Paek

8A.2 - Imprecise Security: Quality and Complexity Tradeoffs for Hardware Information Flow Tracking 674
Wei Hu, Andrew Becker, Armita Ardeshiricham, Yu Tai, Paolo Ienne, Dejun Mu, Ryan Kastner

8A.3 - Encasing Block Ciphers to Foil Key Recovery Attempts via Side Channel 682
Giovanni Agosta, Alessandro Barenghi, Gerardo Pelosi, Michele Scandale

8A.4 - Security of Neuromorphic Computing: Thwarting Learning Attacks Using Memristor’s Obsolescence Effect 690
Chaofei Yang, Beiye Liu, Wujie Wen, Mark Barnell, Qing Wu, Hai Li, Yiran Chen, Jeyavijayan Rajendran

8B.1 - Generation and Use of Statistical Timing Macro-models considering Slew and Load Variability 696
Debjit Sinha, Vladimir Zolotov, Jin Hu, Sheshashayee Raghunathan, Adil Bhanji, Christine Casey

8B.2 - TinySPICE Plus: Scaling Up Statistical SPICE Simulations on GPU Leveraging Shared-Memory Based Sparse Matrix Solution Techniques 702
Lengfei Han, Zhuo Feng

Grace Li Zhang, Bing Li, Ulf Schlichtmann

8B.4 - A Fast Layer Elimination Approach for Power Grid Reduction 716
Abdul-Amir Yassine, Farid Najm

8C.1 - A Deterministic Approach to Stochastic Computation 724
Devon Jenson, Marc Riedel

8C.2 - Control-Fluidic CoDesign for Paper-Based Digital Microfluidic Biochips 732
Qin Wang, Zeyan Li, Hae Na Cheong, Oh-Sun Kwon, Hailong Yao, Tsung-Yi Ho, Kwanwoo Shin, Bing Li, Ulf Schlichtmann, Yici Cai

8C.3 - Neural Networks Designing Neural Networks: Multi-Objective Hyper-Parameter Optimization 740
Sean Smithson, Guang Yang, Warren Gross, Brett Meyer
8C.4 - Error Recovery in a Micro-Electrode-Dot-Array Digital Microfluidic Biochip 748
Zipeng Li, Kelvin Yi-Tse Lai Lai, Po-Hsien Yu, Krishnendu Chakrabarty, Miroslav Pajic, Tsung-Yi Ho, Chen-Yi Lee

8D.1 - Privacy Protection via Appliance Scheduling in Smart Homes 756
Jie Wu, Jinglan Liu, Yiyu Shi, X. Sharon Hu

8D.2 - Framework Designs to Enhance Reliable and Timely Services of Disaster Management Systems 762
Chi-Sheng Shih, Pi-Cheng Hsiu, Yuan-Hao Chang, Shih-Hao Hung, Tei-Wei Kuo

8D.3 - Analysis of Production Data Manipulation Attacks in Petroleum Cyber-Physical Systems 770
Xiaodao Chen, Yuchen Zhou, Hong Zhou, Chaowei Wan, Qi Zhu, Wenchao Li, Shiyan Hu

8D.4 - Security Challenges in Smart Surveillance Systems and the Solutions Based on Emerging Nanodevices 777
Chaofei Yang, Chunpeng Wu, Yiran Chen, Hai Li, Qing Wu, Mark Barnell

9A.1 - Fast Physics-Based Electromigration Checking for On-Die Power Grids 783
Sandeep Chatterjee, Valeriy Sukharev, Farid N. Najm

9A.2 - Exploring Aging Deceleration in FinFET-Based Multi-Core Systems 791
Ermao Cai, Dimitrios Stamoulis, Diana Marculescu

9A.3 - An Efficient and Accurate Algorithm for Computing RC Current Response with Applications to EM Reliability Evaluation 799
Zhong Guan, Malgorzata Marek-Sadowska

9A.4 - Voltage-Based Electromigration Immortality Check for General Multi-Branch Interconnects 805
Zeyu Sun, Erтурغل Demircan, Mehul D. Shroff, Taeyoung Kim, Xin Huang, Sheldon Tan

9B.1 - Exploiting Randomness in Sketching for Efficient Hardware Implementation of Machine Learning Applications 812
Ye Wang, Michael Orshansky, Constantine Caramanis

9B.2 - Making neural encoding robust and energy-efficient: an advanced analog temporal encoder for brain-inspired computing systems 820
Chenyuan Zhao, Jialing Li, Yang Yi

9B.3 - Statistical Methodology to Identify Optimal Placement of On-Chip Process Monitors for Predicting Fmax 826
Szu-Pang Mu, Wen-Hsiang Chang, Yi-Ming Wang, Ming-Tung Chang, Min-Hsiu Tsai, Mango C.T. Chao

9B.4 - BugMD: Automatic Mismatch Diagnosis for Bug Triaging 834
Biruk Mammo, Milind Furia, Valeria Bertacco, Scott Mahlke, Daya Khudia
9C.1 - ODESY: a novel 3T-3MTJ cell design with Optimized area DEnsity, Scalability and latencY  841
Linuo Xue, Yuanqing Cheng, Jianlei Yang, Peiyuan Wang, Yuan Xie

9C.2 - Delay-Optimal Technology Mapping for In-Memory Computing using ReRAM Devices  849
Debjyoti Bhattacharjee, Anupam Chattopadhyay

9C.3 - Reconfigurable In-Memory Computing with Resistive Memory Crossbar  855
Yue Zha, Jing Li

9C.4 - Exploiting Ferroelectric FETs for Low-Power Non-Volatile Logic-in-Memory Circuits  863
Xunzhao Yin, Ahmedullah Aziz, Joseph Nahas, Sumeet Kumar Gupta, Suman Datta, Michael Niemier, Xiaobo Sharon Hu

9D.1 - Approximation Knob: Power Capping Meets Energy Efficiency  871
Anil Kanduri, Mohammad-Hashem Haghbayan, Amir M. Rahmani, Pasi Liljeberg, Axel Jantsch, Nikil Dutt, Hannu Tenhunen

9D.2 - IC Thermal Analyzer for Versatile 3-D Structures Using Multigrid Preconditioned Krylov Methods  879
Scott Ladenheim, Yi-Chung Chen, Milan Mihajlovic, Vasilis Pavlidis

9D.3 - BoostNoC: Power Efficient Network-on-Chip Architecture for Near Threshold Computing  887
Chidhambaranathan Rajamanikkam, Rajesh JayashankaraShridevi, Koushik Chakraborty, Sanghamitra Roy

9D.4 - QScale: Thermally-Efficient QoS Management on Heterogeneous Mobile Platforms  895
Onur Sahin, Aysê K. Coskun

10A.1 - Synthesis of Statically Analyzable Accelerator Networks From Sequential Programs  903
Shaoyi Cheng, John Wawrzynek

10A.2 - Joint Loop Mapping and Data Placement for Coarse-Grained Reconfigurable Architecture with Multi-bank Memory  911
Shouyi Yin, Xianqing Yao, Tianyi Lu, Leibo Liu, Shaojun Wei

10A.3 - Efficient Synthesis of Graph Methods: a Dynamically Scheduled Architecture  919
Marco Minutoli, Vito Giovanni Castellana, Antonino Tumeo, Marco Lattuada, Fabrizio Ferrandi

10B.1 - Tier Partitioning Strategy to Mitigate BEOL Degradation and Cost Issues in Monolithic 3D ICs  927
Sandeep Kumar Samal, Deepak Nayak, Motoi Ichihashi, Srinivasa Banna, Sung Kyu Lim

10B.2 - Cascade2D: A Design-Aware Partitioning Approach to Monolithic 3D IC with 2D Commercial Tools  934
Kyungwook Chang, Saurabh Sinha, Brian Cline, Raney Southerland, Michael Doherty, Greg Yeric, Sung Kyu Lim
10B.3 - SAINT: Handling Module Folding and Alignment in Fixed-outline Floorplans for 3D ICs  942
Jai-Ming Lin, Po-Yang Chiu, Yen-Fu Chang

10C.1 - From Biochips to Quantum Circuits: Computer-Aided Design for Emerging Technologies  949
Robert Wille, Bing Li, Ulf Schlichtmann, Rolf Drechsler

10D.1 - Multilevel Design Understanding: From Specification to Logic  955
Sandip Ray, Ian Harris, Goerschwin Fey, Mathias Soeken