
Samos, Greece
17-21 July 2016
Table of Contents

Keynotes

Potential future research in computing: Heterogeneous systems, memory subsystems - Process-in-Storage, or not to Process-in-Storage? That is the question

Uri Weiser

Is Computer Science Dying?

Alex Nicolau

SESSION 1A: Domain-specific Optimization

Concurrent Memory Subsystem and Application Optimization for ASIP Design ........................................ 1

Juan Fernando Eusse, Francisco Fernandez, Rainer Leupers, and Gerd Ascheid

Automatic Recognition of Computational Kernels for Platform-Dependent Code Optimizations ............... 11

María H. Rodríguez Blanco, Georg Reinke, Gerd Ascheid, and Rainer Leupers

Processes and Actors: Translating Kahn Processes to Dataflow with Firing ............................................ 21

Gustav Cedersjö and Jörn W. Janneck

SESSION 1B: Power & Energy


Connor Imes and Henry Hoffmann

Power Models Supporting Energy-Efficient Co-Design on Ultra-Low Power Embedded Systems ............. 39

Vi Ngoc-Nha Tran, Brendan Barry, and Phuong Hoai Ha

Real-time Tasks and Voltage/Frequency Controller Collaboration on Low Power Energy Operational Systems .... 47

Rawlinson S. Gonçalves, Diego Q. Pinheiro, and Eduardo B. Valentin
# SESSION 3A: System level Performance

<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>numap: A Portable Library For Low-Level Memory Profiling</td>
<td>Manuel Selva, Lionel Morel, and Kevin Marquet</td>
</tr>
<tr>
<td>A Bypass First Policy for Energy-Efficient Last Level Caches</td>
<td>Jason Jong Kyu Park, Yongjun Park, and Scott Mahlke</td>
</tr>
<tr>
<td>Runtime Support for Adaptive Power Capping on Heterogeneous SoCs.</td>
<td>Yun Wu, Dimitrios S. Nikolopoulos, and Roger Woods</td>
</tr>
</tbody>
</table>

# SESSION 3B: Architecture/Processor level Acceleration

<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>AccuRA: Accurate Alignment of Short Reads on Scalable Reconfigurable Accelerators</td>
<td>Santhi Natarajan, Krishna Kumar N, Debnath Pal, and S. K. Nandy</td>
</tr>
</tbody>
</table>

# SESSION 3C: Simulation & Design Space Exploration

<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exploring System Performance using Elastic Traces: Fast, Accurate and Portable</td>
<td>Radhika Jagtap, Stephan Diestelhorst, Andreas Hansson, Matthias Jung, and Norbert When</td>
</tr>
<tr>
<td>CoolSim: Statistical Techniques to Replace Cache Warming with Efficient, Virtualized Profiling</td>
<td>Nikos Nikoleris, Andreas Sandberg, Erik Hagersten, and Trevor E. Carlson</td>
</tr>
<tr>
<td>Architecture Exploration of a Programmable Neural Network Processor for Embedded Systems</td>
<td>Wonyong Sung and Jinhwan Park</td>
</tr>
</tbody>
</table>

# SESSION 3D: System Design

<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supporting Composition in Symbolic System Synthesis</td>
<td>Kai Neubauer, Christian Haubelt, and Michael Glaß</td>
</tr>
<tr>
<td>Design Productivity of a High Level Synthesis Compiler versus HDL</td>
<td>Maxime Pelcat, Cédric Bourrasset, Luca Maggiani, and François Berry</td>
</tr>
<tr>
<td>Multi-View Consistency for Infinitary Regular Languages</td>
<td>Maria Pittou and Stavros Tripakis</td>
</tr>
<tr>
<td>A Configurable SIMD Architecture with Explicit Datapath for Intelligent Learning</td>
<td>Yifan He, Maurice Peemen, Luc Waeijen, Erkan Diken, Mattia Fiumara, Gerard Rauwerda, Henk Corporaal, and Tong Geng</td>
</tr>
</tbody>
</table>
SESSION 3E: Performance Issues in Embedded Systems

Implications of Non-Volatile Memory as Primary Storage for Database Management Systems .......................... 164
   Naveed Ul Mustafa, Adrià Armejach, Ozcan Ozturk, Adrián Cristal, and Osman S. Unsal

Improving Performance in VLIW Soft-core Processors through Software-controlled ScratchPads .................. 172
   Tiago Jost, Gabriel Nazar, and Luigi Carro

NanoStreams: Codesigned Microservers for Edge Analytics in Real Time ...................................................... 180
   Giorgis Georgakoudis, Charles Gillan, Ahmad Hassan, Umar I. Minhas, Ivor Spence, George Tzenakis, Hans
   Vandierendonck, Roger Woods, Dimitrios S. Nikolopoulos, Murali Shyamsundar, Paul Barber, Matthew
   Russell, Angelos Bilas, Stelios Kaloutsakis, Heiner Giefers, Peter Staar, Costas Bekas, Neil Horlock, Richard
   Falcon, and Colin Pattison

Evaluating Physically Unclonable Functions on a large set of FPGAs ......................................................... 188
   Sebastien Bellon, Claudio Favi, Miroslaw Malek, Marco Macchetti, and Francesco Regazzoni

SESSION 3F: Application/Algorithm level Acceleration

Hardware-Efficient Index Mapping for Mixed Radix-2/3/4/5 FFTs ............................................................... 196
   Tomasz Patyk and Jarmo Takala

On the Modeling of Error Functions as High Dimensional Landscapes for Weight Initialization in Learning Networks 202
   Julius, Gopinath Mahale, Sumana T., and C. S. Adityakrishna

Hybrid Code Description for Developing Fast and Resource Efficient Image Processing Architectures ................. 211
   Konrad Häublein, Marc Reichenbach, Oliver Reiche, M. Akif Özkan, Dietmar Fey, Frank Hannig, and Jürgen
   Teich

Automated Dataflow Graph Merging .............................................................................................................. 219
   Nils Voss, Stephen Girdlestone, Oskar Mencer, and Georgi Gaydadjiev

Special Session on Reconfigurable Compute Architectures (RCA)

High-Level Synthesis of Dynamic Dataflow Programs on heterogeneous MPSoC platforms .......................... 227
   Endri Bezati, Simone Casale-Brunet, Marco Mattavelli, and Jörn W. Janneck

Coarse Grained Reconfigurable Architectures in the Past 25 Years: Overview and Classification ...................... 235
   Mark Wijtvliet, Luc Waeijen, and Henk Corporaal

Empowering OpenMP with Automatically Generated Hardware ....................................................................... 245
   Artur Podobas and Mats Brorsson

Aggressively Bypassing List Scheduler for Transport Triggered Architectures ............................................... 253
   Heikki O. Kultala, Timo T. Viitanen, Pekka O. Jääskeläinen, and Jarmo H. Takala

A Hybrid ASIC/FPGA Fault-Tolerant Artificial Pancreas ............................................................................. 261
   Michail Vavouras, Rui Policarpo Duarte, Antonino Armato, and Christos-Savvas Bouganis
Special Session on Circuits, Systems and Design Automation for Emerging Technologies

From Reversible Logic to Quantum Circuits: Logic Design for an Emerging Technology

Robert Wille, Anupam Chattopadhyay, and Rolf Drechsler

A Strong Arbiter PUF using Resistive RAM

Rekha Govindaraj and Swaroop Ghosh

Racetrack Memory-based Encoder/Decoder for Low-Power Interconnect Architectures

Suman Deb, Leibin Ni, Hao Yu, and Anupam Chattopadhyay

Transforming Nanodevices to Next Generation Nanosystems

Max Marcel Shulaker, Gage Hills, H.-S. Philip Wong, and Subhasish Mitra

Special Session on European Projects on heterogeneous microservers and parallel embedded computing

Data Centres for IoT Applications: the M2DC Approach


Performance and Energy evaluation of Spark applications on low-power SoCs

Christoforos Kachris, Ioannis Stamelos, and Dimitrios Soudris

TULIPP: Towards Ubiquitous Low-power Image Processing Platforms

Tobias Kalb, Lester Kalms, Diana Göhringer, Carlota Pons, Fabien Marty, Ananya Muddukrishna, Magnus Jahre, Per Gunnar Kjeldsberg, Boitumelo Ruf, Tobias Schuchert, Igor Tchouchenkov, Carl Ehrenstrahle, Magnus Peterson, Flemming Christensen, Antonio Paolillo, Christian Lemer, Ben Rodriguez, Guillaume Bernard, François Duhem, and Philippe Millet

Performance-Power Exploration of Software-Defined Big Data Analytics: The AEGLE Cloud Backend

Georgios Zervakis, Sotirios Xydis, and Dimitrios Soudris

Safe Cooperative CPS: A V2I Traffic Management scenario in the SafeCOP project

Alessio Agneessens, Francesco Buemi, Stefano Delucchi, Massimo Massa, Giovanni Agosta, Alessandro Barenghi, Carlo Brandolese, William Fornaciari, Gerardo Pelosi, Enrico Ferrari, Dajana Cassioli, Luigi Pomante, Leonardo Napoletani, Luciano Bozzi, Carlo Tieri, and Maurizio Mongelli

Enabling Indoor Object Localization through Bluetooth Beacons on the RADIO Robot Platform

Fynn Schwiegelshohn, Philipp Wehner, Florian Werner, Diana Göhringer, and Michael Hübner
Preface .................................................................................................................. 334
  Michael Hübner and Diana Göhringer Dimitrios Soudris
(Keynote) Perspectives on System-level MPSoC Design Space Exploration .................. 335
  Andy Pimentel
A Framework for Exploring Alternative Fault-Tolerant Schemes Targeting 3-D Reconfigurable Architectures ........... 336
  Kostas Siozios, Ioannis Savidis, and Dimitrios Soudris
MPSoCSim extension: An OVP Simulator for the Evaluation of Cluster-based Multi and Many-core architectures .. 342
  Maria Méndez Real, Philipp Wehner, Jens Rettkowski, Vincent Migliore, Vianney Lapotre, Diana Göhringer, and Guy Gogniat
A Quasi-Cycle Accurate Timing Model for Binary Translation Based Instruction Set Simulators 348
  Sören Schreiner, Ralph Görgen, Kim Grüttner, and Wolfgang Nebel
  Pedro Campos, Nizar Dahir, Colin Bonney, Martin Trefzer, Andy Tyrrell, and Gianluca Tempesti
A Hybrid Approach for Mapping and Scheduling on Heterogeneous Multicore Systems .................. 360
  A. Emeretlis, G. Theodoridis, P. Alefragis, and N. Voros
Black Box ESL Power Estimation for Loosely-Timed TLM Models ........................................ 366
  Gereon Onnebrink, Rainer Leupers, Gerd Ascheid, and Stefan Schürmans
An OpenCL-based Framework for Rapid Virtual Prototyping of Heterogeneous Architectures .............. 372
  Efstathios Sotiriou-Xanthopoulos, Leonard Masing, Kostas Siozios, George Economakos, Dimitrios Soudris, and Jürgen Becker
Incorporating Rapid Design Assembly into a Virtual Prototyping Environment ...................... 378
  Ryan Marlow, Shenghou Ma, Kevin Lee, Andrew Love, and Peter Athanas

Author Index ....................................................................................................... 384