

# **2016 Austrochip Workshop on Microelectronics (Austrochip 2016)**

**Villach, Austria  
19 October 2016**



**IEEE Catalog Number: CFP16AUS-POD  
ISBN: 978-1-5090-1041-7**

**Copyright © 2016 by the Institute of Electrical and Electronics Engineers, Inc  
All Rights Reserved**

*Copyright and Reprint Permissions:* Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

***\*\*\*This publication is a representation of what appears in the IEEE Digital Libraries. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP16AUS-POD
ISBN (Print-On-Demand):	978-1-5090-1041-7
ISBN (Online):	978-1-5090-1040-0

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

CURRAN ASSOCIATES INC.  
**proceedings**  
.com

# 2016 24th Austrian Workshop on Microelectronics

## Austrochip 2016

### Table of Contents

Message from Organizing Committee.....	vii
Workshop Organization.....	viii
Patrons.....	ix
Technical Co-sponsors.....	xvii
Keynote.....	xviii

---

### Analog and Power Management

Advanced Pseudo Differential Amplifier with Output Common Mode Regulation and Phase Shift Retention .....	1
<i>Sagarika Donepudi, Michael Köberle, and Wolfgang Horn</i>	
Modeling and Simulation of Digital Control Schemes for Two-Phase Interleaved Buck Converters .....	7
<i>Marc Kanzian, Matteo Agostinelli, and Mario Huemer</i>	
High-Efficiency CMOS Buck Converter with Wide Output Voltage Range .....	13
<i>Nataša Mitrović, Reinhard Enne, and Horst Zimmermann</i>	
A 11-Bit Integrating Analog to Digital Converter .....	19
<i>Darshan Shetty and Pratap Tumkur Renukaswamy</i>	

### RF and Analog

Analysis and Design of Differential Feedback CG LNA Topologies for Low Voltage Multistandard Wireless Receivers .....	24
<i>Pratap Tumkur Renukaswamy, Vijaya Pasupureddi, and Johannes Sturm</i>	
Threshold Voltage Compensated RF-DC Power Converters in a 40 nm CMOS Technology.....	30
<i>Lukas Zöescher, Peter Herkess, Jasmin Grosinger, Ulrich Muehlmann, Dominik Amschl, Hubert Watzinger, and Wolfgang Böesch</i>	
System-in-Package Matching Network for RF Wireless Transceivers .....	35
<i>Graciele Batistell, Timo Holzmann, Hermann Sterner, and Johannes Sturm</i>	
A Capacitance-to-Digital Converter Based on a Ring Oscillator with Flicker Noise Reduction .....	40
<i>Andres Quintero, Fernando Cardes, Luis Hernandez, Cesare Buffa, and Andreas Wiesbauer</i>	

## **Embedded Systems and Digital**

On Analysis of Software Interrupt Limiters for Embedded Systems by Means of UPPAAL SMC .....	45
<i>Josef Strnadel and Michal Riša</i>	
A Programmable Delay Line for Metastability Characterization in FPGAs .....	51
<i>Thomas Polzer, Florian Huemer, and Andreas Steininger</i>	
An EMI Receiver Model to Minimize Simulation Time of Long Data Transmissions .....	57
<i>Herbert Hackl and Bernd Deutschmann</i>	
<b>Author Index</b> .....	63