2016 29th IEEE International System-on-Chip Conference (SOCC 2016)

Seattle, Washington, USA
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2016 29th IEEE International System-on-Chip Conference (SOCC)

Best Paper Award I

Shu Hokimoto, Tohru Ishihara and Hidetoshi Onodera (Kyoto University, Japan)

11:45 Digital LDO Modeling for Early Design Space Exploration
Stefan Leitner (Southern Illinois University Carbondale); Paul West, Chao Lu and Haibo Wang (Southern Illinois University Carbondale, USA)

12:10 A Digital-circuit-based Evolutionary-computation Algorithm for Time-interleaved ADC Background Calibration
Dadian Zhou (Texas A&M University, USA); Claudio Talarico (Gonzaga University, USA); Jose Silva-Martinez (Texas A&M University, USA)

RF, Analog Design I

11:20 Area-Power-Efficient 11-Bit Hybrid Dual-Vdd ADC with Self-Calibration for Neural Sensing Applications
Jr-Ming Chen (Nation Chiao Tung University, Taiwan); Po-Tsang Huang (National Chiao Tung University); Shang-Lin Wu(Nation Chiao Tung University, Taiwan); Wei Hwang and Ching-Te Chuang (National Chiao Tung University, Taiwan)

11:45 A 12 Bit Split-Array Switched Capacitor Power Amplifier in 130nm CMOS
Zhidong Bai, Ali Azam, Dallas Johnson, Wen Yuan and Jeffrey Walling (University of Utah, USA)

12:10 Low-Jitter All-Digital Phase-Locked Loop with Novel PFD and High Resolution TDC & DCO
Xiaoying Deng, Yanyan Mo, Xin Lin and Mingcheng Zhu (Shenzhen University, P.R. China)

SoC Design Methods and Algorithms I

14:00 Statistical Design Attribute Identification for FinFET Outlier and Silicon-to-SPICE Gap
Hyosig Won and Katsuhiro Shimazu (Samsung Electronics, Korea)

14:25 Intra-chip Traffic Generation Under Autoregressive Models Based on Time Series Obtained by TLM Simulation
Jose E Bueno (University of Sao Paulo, Brazil); Jorge Gonzalez (University of Campinas, Brazil); Wang Chau (University of Sao Paulo)

14:50 A Method to Estimate Effectiveness of Weak Bit Test: Comparison of Weak pMOS and WL Boost Based Test - 28nm FDSOI Implementation
Nidhi Batra, Shashwat Kaushik and Anil Gundu Kumar (IIIT Delhi, India); Mohammad Hashmi (IIIT Delhi); Anuj Grover(ST Microelectronics, India); Gangaikondan Visweswaran (IIIT Delhi, India)

15:15 CATBR-Congestion Aware Traffic Bridging Routing Among Hierarchical Networks-on-Chip
Mingmin Bai (University of Louisiana at Lafayette, USA); Danella Zhao (Old Dominion University, USA); Hongyi Wu(University of Louisiana at Lafayette, USA)
**Special Session: Emerging Trends in SoC Testing**

14:00 *EDT Dynamic Bandwidth Management in SoC Testing*
Yu Huang (Mentor Graphics, USA)

14:25 *Toward More Efficient Scan Data Bandwidth Utilization on Modern SOCs*
Grady Giles (AMD); GuoLiang Li (AMD, P.R. China); Jeff Rearick, John Schulze, James Wingfield, Tim Wood and Yan Dong (AMD, USA)

14:50 *In-Field System-Health Monitoring Based on IEEE 1687*
Farrokh Ghani Zadegan, Dimitar Nikolov and Erik Larsson (Lund University, Sweden)

**Application Specific SoC Designs**

16:00 *Novel Lightweight FF-APUF Design for FPGA*
Chongyan Gu (Queen's University Belfast, United Kingdom); Yijun Cui (Nanjing University of Aeronautics and Astronautics, P.R. China); Neil Hanley and Maire O'Neill (Queen's University Belfast, United Kingdom)

16:25 *Efficient VLSI Architecture for SAO Decoding in 4K Ultra-HD HEVC Video Codec*
Mihir N Mody, Niraj Nandan and Hetul Sanghvi (Texas Instruments, Inc.)

16:50 *A Flexible Router Architecture for Three-Dimensional Network-on-Chips*
Mostafa Khamis (Mentor Graphics Egypt, Egypt); Mostafa Said Abdelrehim (Sun Yat-sen University-Carnegie Mellon University (SYSU-CMU) Joint Institute of Engineering, Guangzhou, China); Ahmed Shalaby (Egypt Japan University for Science and Technology, Egypt)

17:15 *Single-ended D Flip-Flop with Implicit Scan Mux for High Performance Mobile AP*
Min Su Kim, Chung-Hee Kim, Yong-geol Kim, Ah-Reum Kim, Jikyum Kim, Juhyun Kang, Daeseong Lee, Changjun Choi, Isuk Suh, Youngmin Shin and Jae Cheol Son (Samsung Electronics Inc., Korea)

**Emerging and Evolutionary Design Algorithms**

16:00 *Multi-Objective Sample Preparation Algorithm for Microfluidic Biochips Supporting Various Mixing Models*
Yung-Chun Lei (National Chiao Tung University, Taiwan); Tung-Hsuan Lin (MediaTek Inc., Taiwan); Juinn-Dar Huang (National Chiao Tung University, Taiwan)

16:25 *A Multiplication Reduction Technique with Near-Zero Approximation for Embedded Learning in IoT Devices*
Yuxiang Huan (Fudan University); Yifan Qin (Fudan University, P.R. China); Yantian You (KTH-The Royal Institute of Technology); Lirong Zheng (Fudan University, P.R. China); Zhuo Zou (KTH-The Royal Institute of Technology, Sweden)

16:50 *Feature Study on a Programmable Network Traffic Classifier*
Keissy Guerra Perez (Queen University of Belfast, United Kingdom); Xin Yang and Sandra Scott-Hayward (Queen's University Belfast, United Kingdom); Sakir Sezer (Queen's University Belfast & CTO Titan IC, United Kingdom)

17:15 *Design and ASIC Acceleration of Cortical Algorithm for Text Recognition*
Sumon Dey and Paul Franzon (North Carolina State University, USA)
Poster Session & Reception

A 200 MS/s 8-bit Time-Based Analog-to-Digital Converter with Inherit Sample and Hold
Ali H. Hassan (Cairo University); Mohammed Ismail (Cairo University, Egypt); Yehea Ismail (American University in Cairo, USA); Hassan Mostafa (University of Toronto, Canada)

A 0.4V 320Mb/s 28.7μW 1024-bit Configurable Multiplier for Subthreshold SOC Encryption
Weiwei Shi (Shenzhen University & The Chinese University of Hong Kong, P.R. China); Chiu-sing Oliver Choy (The Chinese University of Hong Kong)

Low Voltage Flash Memory Design Based on Floating Gate SOFFET
Emeshaw Ashenafi (University of Missouri-Kansas City, USA); Azzedin Es-Sakhi (University of Missouri – Kansas City, USA); Masud H Chowdhury (University of Illinois at Chicago, USA)

Hardware Implementation of Hierarchical Temporal Memory Algorithm
Weifu Li and Paul Franzon (North Carolina State University, USA)

An Early Global Routing Framework for Uniform Wire Distribution in SoCs
Bapi Kar (Indian Institute of Technology, Kharagpur); Susmita Sur-Kolay (ISI Kolkata, India); Chittaranjan Mandal (Indian Institute of Technology, Kharagpur, India)

SAMi: Self-Aware Migration Approach for Congestion Reduction in NoC-based MCSoC
Amin Rezaei (University of Louisiana at Lafayette, USA); Masoud Daneshtalab (KTH Royal Institute of Technology, Sweden); Danella Zhao (Old Dominion University, USA); Mehdi Modarressi (University of Tehran, Iran)

Modeling and Optimization of the Bond-Wire Interface in a Hybrid CMOS-Photonic Traveling-Wave MZM Transmitter
Kehan Zhu, Vishal Saxena and Xinyu Wu (Boise State University, USA)

A Jitter Cancellation Circuit for High Speed I/O Interfaces
Anupjyoti Deka and Mahalingam Nagarajan (Intel, India)

A CMOS Analog Front-End for Driving a High-Speed SAR ADC in Low-Power Ultrasound Imaging Systems
Taehoon Kim, Han Yang, Sangmin Shin, Hyongmin Lee and Suhwan Kim (Seoul National University, Korea)

Behavioral Modeling of Drain Current of an Avalanche ISFET Near Breakdown Voltage
Mohammad Uzzal and Payman Zarkesh-Ha (University of New Mexico, USA); Paul Szauter (ElectroSeq); Jeremy Edwards (University of New Mexico)

A Novel Power Reduction Technique Using Wire Multiplexing
Mostafa Said Abdelrehim (Sun Yat-sen University-Carnegie Mellon University (SYSU-CMU) Joint Institute of Engineering, Guangzhou, China); Hossam Hassan and HyungWon Kim (Chungbuk National University & College of Electrical and Computer Engineering, Korea)

An Ultra-Low Power Voltage-to-Time Converter (VTC) Circuit for Low Power and Low Speed Applications
Hassan Mostafa (University of Toronto, Canada); Ali H. Hassan (Cairo University); Tawfik Ismail (NILES, Cairo University, Egypt); Salam Gabran (University of Waterloo, Canada)

Automated Full Chip SPICE Simulations with Self-Checking Assertions for Last Mile Verification & First Pass Silicon of Mixed Signal SoCs

Gautham Shivender Harinarayan, Manmohan Rana, Nitin Pant, Manish Bansal, Sarthak Sharma and Nishant Kaundal (Freescale Semiconductor India (NXP), India)

Analytical Noise Model for Avalanche ISFET Sensor Suitable for Next Generation Sequencing
Mohammad Uzzal and Payman Zarkesh-Ha (University of New Mexico, USA); Paul Szauter (ElectroSeq); Jeremy Edwards (University of New Mexico)

Rotator-Based Multiplexer Network Synthesis for Field-Data Extractors
Koki Ito and Kazushi Kawamura (Waseda University, Japan); Yutaka Tamiya (Fujitsu Laboratories Ltd., Japan); Masao Yanagisawa and Nozomu Togawa (Waseda University, Japan)

A Comparator Timing Assisted SAR ADC Technique with Reduced Conversion Cycles
Abhilash Karnatakam Nagabhushana (Southern Illinois University Carbondale); Haibo Wang (Southern Illinois University Carbondale, USA)

Efficient Implementation of the AES Algorithm for Security Applications
Shady Soliman, Mohamed Abdel Ghany and Baher Magdy (GUC, Egypt)

High-Voltage Low-Power Startup Backup Battery Switch Using Low Voltage Devices in 28nm CMOS
Filippo Maria Neri (U-blox AG); Craig Keogh (U-blox AG, Switzerland); Thomas Brauner and Eric De Mey (U-blox AG); Christian Schippel (Globalfoundries, Germany)

Best Paper Award II

10:45 Design of a Power-Efficient ARM Processor with a Timing-Error Detection and Correction Mechanism
Sao-Jie Chen, Grace Liu, Hsin-Ping Yang and Cheng-Hao Luo (National Taiwan University, Taiwan); Wen-Mei Hwu (University of Illinois at Urbana-Champaign, USA)

11:10 Compressive Image Sensor Technique with Sparse Measurement Matrix
Stefan Leitner (Southern Illinois University Carbondale); Haibo Wang (Southern Illinois University Carbondale, USA); Spyros Tragoudas (Southern Illinois University, Carbondale, USA)

11:35 Performance Optimization and Power Efficiency in 3D IC with Buffer Insertion Scheme
Mohammad Ahmed, Sucheta Mohapatra and Malgorzata Chrzanowska-Jeske (Portland State University, USA)

Special Session: SoC Architectures for Machine Learning through Inexactness

11:05 CaPSuLe: A Camera-based Positioning System Using Learning
Yongshik Moon, Soonhyun Noh and Daedong Park (Seoul National University, Korea); Chen Luo and Anshumali Shrivastava (Rice University, USA); Seongsoo Hong (Seoul National University, Korea); Krishna Palem (Rice University, USA)

11:25 Overcoming the Power Wall by Exploiting Inexactness and Emerging COTS Architectural Features Trading Precision for Improving Application Quality
Mike Fagan (Rice University, USA); Jeremy Schlacter (Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland); Kazutomo Yoshii and Sven Leyffer (Argonne National Laboratory, USA); Krishna Palem (Rice University, USA); Marc Snir (Argonne National Laboratories, USA); Stefan Wild (Argonne National Laboratory, USA); Christian Enz (EPFL, Switzerland)

11:45 Low-Power Real-Time Intelligent SoCs for Smart Machines
**Advanced SoC Components**

13:30 *Standard Cell Library Based Layout Characterization and Power Analysis for 10nm Gate-All-Around (GAA) Transistors*

Youchang Kim, Injoon Hong and Seongwook Park (Korea Advanced Institute of Science and Technology (KAIST), Korea); Hoi-Jun Yoo (Korea Advanced Institute of Science and Technology, Korea)

13:55 *Comparative Analysis of Hybrid Magnetic Tunnel Junction and CMOS Logic Circuits*

Luhao Wang, Tiansong Cui and Shahin Nazarian (University of Southern California, USA); Yanzhi Wang (Syracuse University, USA); Massoud Pedram (University of Southern California, USA)

14:20 *Modeling and Simulation of Quantum-Well Infrared Photodetectors*

Darya Almasi (San Francisco State University, USA); Houman Homayoun (George Mason University, USA); Hassan Salmani (Howard University, USA); Hamid Mahmoodi (San Francisco State University, USA)

14:45 *Sensitivity Analysis for SoC Performance Benchmark Against Interconnect Parasitic Resistance and Capacitance Beyond 10-nm FinFET Technology*

Motoi Ichihashi, Jia Zeng, Cole Zemke, Irene Lin, Greg Northrop, Ning Jin and Jongwook Kye (Globalfoundries, USA)

**RF, Analog Design II**

13:30 *A Low Power Fourth Order ΣΔ CMOS Modulator with Subthreshold Amplifier*

Kwang S. Yoon and Jae-Hyeon Seong (Inha University, Korea); Soo-Hun Yang (Silicon Works, Korea)

13:55 *A Novel Design of a Dual Functionality Read-Write Driver for SRAM*

Pulkit Sharma (IIITD); Mohammad Hashmi (IIITD, India)

14:20 *Novel Ultra Low Voltage Mobile Compatible RF MEMS Switch for Reconfigurable Microstrip Antenna*

Hassan Mostafa (University of Toronto, Canada); Moez El-Massry and Moataz M. Medhat (Cairo University, Egypt)

**SoC Design Methods and Algorithms II**

08:30 *Heterogeneous Memory Assembly Exploration Using a Floorplan and Interconnect Aware Framework*

Prakhar Raj Gupta (Indian Institute of Technology, Delhi & ST Microelectronics India, India); Gaurav Narang (STMicroelectronics, India); Gangaikondan Visweswaran (Indian Institute of Technology, Delhi); Anuj Grover (ST Microelectronics, India)

08:55 *Variable-Length VLIW Encoding for Code Size Reduction in Embedded Processors*

Ting-Yu Shyu (National Chung Cheng University); Bo-Yu Su and Tay-Jyi Lin (National Chung Cheng University, Taiwan); Chingwei Yeh (National Chung-Cheng University, Taiwan); Tien-Fu Chen (National Chiao Tung University, Taiwan); Jinn-Shyan Wang (National Chung Cheng University, Taiwan)

09:20 *Self-dual Diamond-graph CMOS H-bridge Logic Family*

Shun-Wen Cheng (Far East University, Taiwan)
09:45 **ERFAN: Efficient Reconfigurable Fault-Tolerant Deflection Routing Algorithm for 3-D Network-on-Chip**
Somayeh Maabi (Shahid Beheshti University, Iran); Farshad Safaei (Shahid Beheshti University, Iran); Amin Rezaei (University of Louisiana at Lafayette, USA); Masoud Daneshtalab (KTH Royal Institute of Technology, Sweden); Danella Zhao (Old Dominion University, USA)

Special Session: Emerging Stochastic Computing and Neuromorphic Computing: Arithmetic, Algorithm, and Applications

08:30 **Design of High-speed Low-power Polar BP Decoder Using Emerging Technologies**
Ao Ren (Syracuse University, USA); Bo Yuan (City University of New York, USA); **Yanzhi Wang** (Syracuse University, USA)

08:55 **A Low-Computation-Complexity, Energy-Efficient, and High-Performance Linear Program Solver Using Memristor Crossbars**
Ruizhe Cai, Ao Ren, **Yanzhi Wang**, Sucheta Soundarajan and Qinru Qiu (Syracuse University, USA); Bo Yuan (City University of New York, USA); Paul Bogdan (University of Southern California, USA)

09:20 **Efficient Hardware Architecture of Softmax Layer in Deep Neural Network**
Bo Yuan (City University of New York, USA)

09:45 **Noisy Neuromorphic Circuit Modeling Obsessive Compulsive Disorder**
Saeid Barzegarjalal, Kun Yue and Alice C. Parker (University of Southern California, USA)

Low Power Design

10:30 **Practical Power Consumption Analysis with Current Smartphones**
Xiang Chen (George Mason University, USA); Kent Nixon and Yiran Chen (University of Pittsburgh, USA)

10:55 **Fully Parallel Content Addressable Memory Design Using Multi-Bank Structure**
Shixiong Jiang (University at Buffalo, USA); Vijayalakshmi Saravanan (University at Buffalo); Pengzhan Yan and Ramalingam Sridhar (University at Buffalo, USA)

11:20 **New Power Budgeting and Thermal Management Scheme for Multi-Core Systems in Dark Silicon**
Hai Wang and Ming Zhang (University of Electronic Science and Technology of China, P.R. China); Sheldon Tan (University of California, Riverside, USA); Chi Zhang and Yuan Yuan (University of Electronic Science and Technology of China, P.R. China); Keheng Huang and Zhenghong Zhang (Southwest China Research Institute of Electronic Equipment, P.R. China)

11:45 **Overoptimistic Voltage Scaling in Pre-Error AVS Systems and Learning-Based Alleviation**
Yi-Hsuan Ting (National Chung Cheng University, Taiwan); Chih-Yang Wang (National Tsing Hua University, Taiwan); Yu-Sian Chang (National Chung Cheng University, Taiwan); Tay-Jyi Lin (National Chung Cheng University, Taiwan); Shih-Chieh Chang (National Tsing Hua University); Jinn-Shyan Wang (National Chung Cheng University, Taiwan)

Special Session: Security and Validation in Mobile, Embedded, and IoT Systems

10:30 **Security Challenges in Mobile and IoT Systems**
Sandip Ray (NXP Semiconductors, USA); Jayanta Bhadra (NXP Semiconductors)
10:50 Quantifying Trust in Autonomous System Under Uncertainties
Raj Gautam Dutta, Xiaolong Guo and Yier Jin (University of Central Florida, USA)

11:10 Striking a Balance Between SoC Security and Debug Requirements
Wen Chen and Jayanta Bhadra (NXP Semiconductor, USA)