2016 20th International Symposium on VLSI Design and Test (VDAT 2016)

Guwahati, India
24-27 May 2016
**Track-wise list of papers**

**Session 1A- Memory**

Variability and Reliability aware Surrogate Model for Sensing Delay analysis of SRAM Sense Amplifier  
  *Sapna Khandelwal, Jyoti Meena, Lokesh Garg and Dharmendar Boolchandani*

Modeling and Yield Optimization of SRAM Sub-System for Different Capacities Subjected to Parametric Variations  
  *Pulkit Sharma, Anil Kumar Gundu and Mohammad S Hashmi*

A High Speed Low Voltage Latch Type Sense Amplifier for Non-Volatile Memory  
  *Disha Arora, Anil Gundu and Mohammad Hashmi*

**Session 1B-Digital**

BDD based Synthesis Technique for Design of High-Speed Memristor based Circuits  
  *Anindita Chakraborty, Rakesh Das, Chandan Bandyopadhyay and Hafizur Rahaman*

High Performance Bit-Sliced Pipelined Comparator Tree for FPGAs  
  *Ayan Palchaudhuri and Anindya Sundar Dhar*

T-Gate: Concept of partial polarization in Quantum dot Cellular Automata  
  *Chiradeep Mukherjee, Soudip Sinha Roy, Saradindu Panda and Prof. Dr. Banshibadan Maji*

**Session 2A-RF**

Backward Compatible Mil-STD-1553B Analog Transceiver Upgrade for 100-Mb/S Data Rate  
  *Prateek Pendyala and Vijaya Sankara Rao Pasupureddi*

Design And Measurement Techniques For A Low Noise Amplifier In A Receiver Chain For MedRadio Spectrum Of 401-406 MHz Frequency Band  
  *Abhishek Srivastava, Nithin Sankar K, Rakesh K K, Baibhab Chatterjee, Devarshi Das and Maryam Shojaei Baghini*

New technique to improve transient response of LDO regulators without an off-chip capacitor  
  *Chetan Parikh and Gopal Agarwal*

**Session 2B-Verification**

A FSM Based Approach for Efficient Implementation of K-Means Algorithm  
  *Rahul Ratnakumar and Satyasai Jagannath Nanda*

An Effective and Efficient Algorithm to Analyse and Debug Clock Propagation Issues  
  *Akhilesh Chandra Mishra, Aditi Sharma, Sakshi Gupta, Pawan Sehgal and Sujay Deb*

Design of Coherence Verification Unit for CMPs Realizing Dragon Protocol
Biddesh Chakraborty, Mamata Dalui and Biplab K Sikdar

Guided Shifting of Test Pattern to Minimize Test Time in Multiple Serial Scan

Jaynarayan Tudu and Satyadev Ahlawat

Session 3A-Devices & Technology

A Unified Verilog-A Compact Model for Lateral Si Nanowire (NW) FET Incorporating Parasitics for Circuit Simulation

Om Prakash, Dr. Satish Maheshwaram, Mohit Sharma, Anand Bulusu, Ashok Kumar Saxena and Sanjeev Manhas

Frequency Domain Analysis of On-Chip Power Distribution Network

Shipra Batra, Pankhuri Singh, Shashwat Kaushik and Mohammad S. Hashmi

Density Gradient Quantum Corrections based Performance Optimization of Triangular TG Bulk FinFETs using ANN and GA

Ankit Gaurav, Sandeep Gill, Navneet Kaur and Munish Rattan

Session 3B- Embedded

PGA Implementation of High Speed Reconfigurable Filter Bank for Multi-standard Wireless Communication Receivers

Sasha Garg and Sumit Darak

Synthesis of Scheduler Automata Guaranteeing Stability and Reliability of Embedded Control Systems

Saurav Kumar Ghosh, Akash Mondal, Souradeep Dutta, Aritra Hazra and Soumyajit Dey

An Efficient FPGA-Based Function Profiler for Embedded System Applications

Pavan Kumar Nadimpalli and Subir K Roy

Session 4A-Memory

A Robust 8T FinFET SRAM Cell with Improved Stability for Low Voltage Applications

C B Singh Kushwah, Devesh Dwivedi and Krisnan S Rengrajan

New Stable Loadless 6T Dual Port SRAM Cell Design

Antara Ganguly, Sangeeta Goyal, Sneha Bhatia and Anuj Grover

Session 4B-Digital

Analysis of Regeneration Time Constant of Dynamic Latch using Adomian Decomposition Method

Purushothaman A.

An Area and Performance Aware ECG Encoder Design for Wireless Healthcare Services

Bharat Garg, Sameer Yadav and G K Sharma

Efficient Implementation of Concurrent Lookahead Decision Feedback Equalizer using Offset Binary Coding

Mohd Tasleem Khan, Rafi Ahamed Shaik and Amitabh Chatterjee
Session 5A- Analog

A Method To Design A Comparator For Sampled Data Processing Applications
Ram Prasad Acharya, Abir J Mondal and Alak Majumder

Performance Analysis of Temperature Dependent GNR Interconnect
Waikhom Mona Chanu, Vikash Prasad and Debaprasad Das

Switched Capacitor Circuit Simulator In Q-V Domain Including Non Idealities
Muralidhar Gadamsetty, G Dinesh and Binsu Kailath

Session 5B- Testing

JSCAN: A Joint-scan DFT Architecture to Minimize Test Time, Data Volume, and Test Power
Jaynarayan Tudu

Approximate Conditional Carry Adder for Error Tolerant Applications
Avishek Sinha Roy, N Prasad and Anindya Sundar Dhar

An Effective Test Methodology Enabling Detection of Weak bits in SRAMs: Case Study in 28nm FDSOI
Nidhi Batra, Anil Gundu Kumar, Anuj Grover, Mohammad S Hashmi and Gangaikondan Subramani Visweswaran

Skip-Scan: A Methodology for Test Time reduction
Binod Kumar, Boda Nehru, Brajesh Pandey and Jaynarayan Tudu

Session 6A-Systems

Towards A Dynamic Associativity Enabled Write Prediction Based Hybrid Cache
Sukarn Agarwal and Hemangee K. Kapoor

Cognitive-Radio Wireless-Sensor based on Energy Detection with Improved Accuracy: Performance and Hardware Perspectives
Rahul Shrestha, Vinay Swargam and Mahesh Murty

Synthesis Aware Sample Preparation Techniques Using Random Sample Sets in DMFB
Pranab Roy, Sudeshna Chakraborty, Hafizur Rahaman and Parthasarathi Dasgupta

Pre-Layout Module wise decap allocation for Noise suppression and Accurate Delay estimation of SoC
Moumita Chakraborty, Amlan Chakrabarti, Partha Mitra, Debasri Saha and Krishnendu Guha

Session 7A-Security & CAD

An Efficient Reversible Cryptographic Circuit Design
Bikromadittya Mondal, Kushal Dey and Susanta Chakraborty

Double Patterning Lithography (DPL)-Compliant Layout Construction (DCLC) with Area-Stitch
usage tradeoff

Debasis Pal, Abir Pramanik, Parthasarathi Dasgupta and Debesh Kumar Das

A Pre-RTL Floorplanner Tool for Automated CMP Design Space Exploration with Thermal Awareness

Sri Harsha Gade, Praveen Kumar and Sujay Deb

Hardware Optimizations for Crypto Implementations (Invited Paper)

Mohamed Asan Basiri M and Sandeep K. Shukla

Session 7B-Low Power

On Minimization of Test Power through Modified Scan Flip-Flop

Satyadev Ahlawat and Jaynarayan T Tudu

Guided Multilevel Approximation of Less Significant Bits for Power Reduction

Celia Dharmaraj and Nitin Chandrachoodan

SAT: A New Application Mapping Method for Power Optimization in 2D – NoC

Aravindhan Alagarsamy and Lakshminarayanan G.

On Determination of Instantaneous Peak and Cycle Peak Switching using ILP

Rohini Gulve, Nihar Hage and Jaynarayan T Tudu

Session 8A-Analog

A Constraint Driven Technique For MOS Amplifier Design

Paromita Bhattacharjee, Abir J Mondal and Alak Majumder

Programmable Output Switched Capacitor Step-down DC-DC Converter with High Accuracy using Sigma-Delta Feedback Control Loop

Mahesh Zanwar and Subhajit Sen

Design Methodology of Closed Loop MEMS Capacitive Accelerometers based on ΣΔ Modulation Technique

Procheta Chatterjee, Sougata Kar and Siddhartha Sen

Optimal Design Flow of CMOS Doubler-based Rectifiers

Soumik Sarkar, Gaurav Saini, Mahima Arrawatia and Maryam Shojaei Baghini.

Session 8B- Systems

Tag Only Storage for Capacity Optimised Last Level Cache in Chip Multiprocessors

Surajit Das, Shirshendu Das and Hemangee K. Kapoor

Planning based Guided Reconstruction of Corner Cases in Architectural Validation

Rajib Lochan Jana, Soumyajit Dey, Pallab Dasgupta, Shashank Kuchibhotla and Rakesh Kumar

A Low-Cost Energy Efficient Image Scaling Processor for Multimedia Applications

Bharat Garg, V N S K Chaitanya Goteti and G K Sharma
EG0N: Portable In-Situ Energy Measurement for Low-Power Sensor Devices  
Nils Heitmann, Philipp Kindt and Samarjit Chakraborty

Papers for interactive session/short papers

A High CMRR, High Resolution bio-ASIC for ECG Signals
Kiran Garje, Shravan Kumar, Amitesh Tripathi, Maruthi G and Madhav Kumar M. A High CMRR

Temperature Dependent IR-Drop and Delay Analysis in Side-Contact Multilayer Graphene Nanoribbon Based Power Interconnects
Sandip Bhattacharya, Debaprasad Das and Hafizur Rahaman

Design, Integration and Performance Analysis of ΣΔ ADC for Capacitive Sensor Interfacing
Procheta Chatterjee, Sougata Kar, Dushyant Juneja and Siddhartha Sen

A Strategy for Fault Tolerant Reconfigurable Network-on-Chip Design
Navonil Chatterjee, Priyajit Mukherjee and Santanu Chattopadhyay

Formal Verification of Switched Capacitor DC to DC Power Converter Using SPICE Circuit Simulation Traces
Ambuj Mishra and Subir Kumar Roy

Golden IC free Methodology for Hardware Trojan Detection using Symmetric Path Delays
Ramakrishna Vaikuntapu, Lava Bhargava and Vineet Sahula

FFT/IFFT implementation using Vivado HLS
Amit Salaskar and Nitin Chandrachoodan

Reducing FIFO Buffer Power Using Architectural Alternatives at RTL
Ashish Sharma, Manoj Singh Gaur, Lava Bhargava, Vijay Laxmi and Ruby Ansar

Data Dependent Suprious Power Reduction for FWM
Bharti Navlani, Pankaj U. Joshi and Raghavendra Deshmukh

A Mismatch Insensitive Reconfigurable Discrete Time Biosignal Conditioning Circuit in 180 nm MM CMOS Technology
Priyanka Kimtee, Devarshi Mrinal Das and Maryam Shojaei Baghini

Quantification of figures of merit of 7T and 8T SRAM cell in sub-threshold region and their comparison with the conventional 6T SRAM cell
Pulkit Sharma, Jasmine Kaur Gulati, K. Bharath, Renduchinthala Anusha, Preet Kaur Walia and Sumit Darak

A Low Power High Speed Hybrid Full Adder
Manan Mewada and Mazad Zaveri

FSK Demodulator And FPGA Based BER Measurement System For Low IF Receivers
Nithin Sankar K, Abhishek Srivastava, Baibhab Chatterjee, Rakesh K K and Maryam Shojaei Baghini
Energy-efficient Reconfigurable Framework for Evaluating Hybrid NoCs
Raghav Kishore, Hemanta Kumar Mondal and Sujay Deb

An 8-bit 500 MSPS Segmented Current Steering DAC using Chinese Abacus Technique
Sachin Khandagale and Santanu Sarkar

A Novel Low power 6-bit FLASH ADC using Charge steering amplifier For RF Application
Krishna Kumar Movva and Azeemuddin Syed

Design of Fault Tolerant Majority Voter for TMR Implementation in QCA
Subrata Chattopadhyay, Shiv Bhushan Tripathi, Mrinal Goswami and Bibhash Sen

Smart Handheld Platform For Electrochemical Bio Sensors
Suraj Hebbar, Vinay Kumar, M S Bhat and Navakanta Bhat