2017 International Conference on Field Programmable Technology (ICFPT 2017)

Melbourne, Australia
11 – 13 December 2017
1. Architecture

1  RBSA: Range-Based Simulated Annealing for FPGA Placement  
(Junqi Yuan, Lingli Wang, Xuegong Zhou, Yinshui Xia, Jianping Hu)

9  Automatic Circuit Design and Modelling for Heterogeneous FPGAs  
(Sadegh Yazdanshenas, Vaughn Betz)

17  Liquid: High Quality Scalable Placement for Large Heterogeneous FPGAs  
(Dries Vercruyce, Elias Vansteenkiste, Dirk Stroobandt)

25  Performance Characterization of Altera and Xilinx 28nm FPGAs at Cryogenic Temperatures  
(Harald Homulle, Edoardo Charbon)

2. Memory & I/O

32  High Performance Serial ATA Gen3 Controllers on FPGA Devices  
(Dan Cristian Turicu, Octavian Cret, Lucia Vǎcaru)  

40  SMEFF: A Scalable Memory Extension Fabric for FPGA  
(Wei Li, Yangyang Zhao, Yuhang Liu, Mingyu Chen)

48  AXI Over Ethernet; A Protocol for the Monitoring and Control of FPGA Clusters  
(William Kamp)

56  Ultra-Low Latency Continuous Block-Parallel Stream Windowing Using FPGA On-Chip Memory  
(Justin S.J. Wong, Runbin Shi, Maolin Wang, Hayden Kwok-Hay So)

3. Libraries & Synthesis

64  HopliteRT: An Efficient FPGA NoC for Real-Time Applications  
(Saud Wasly, Rodolfo Pellizzoni, Nachiket Kapre)

72  ARCHITECT: Arbitrary-Precision Constant-Hardware Iterative Compute  
(He Li, James J. Davis, John Wickerson, George A. Constantinides)

80  A State Machine Block for High-Level Synthesis  
(Shadi Assadikhomami, Jennifer Ongko, Tor M. Aamodt)

88  An IP Core Integration Tool-Flow for Prototyping Software-Defined Radios Using Static Dataflow with Access Patterns  
(Lekhobola J. Tsoeunyane, Simon Winberg, Michael Inggs)

4. Productivity & Tooling

96  Synthesis of Program Binaries into FPGA Accelerators with Runtime Dependence Validation  
(Shaoyi Cheng, Qijing Huang, John Wawrzynek)

104  Pass a Pointer: Exploring Shared Virtual Memory Abstractions in OpenCL Tools for FPGAs  
(Felix Winterstein, George A. Constantinides)

112  Single Window Stream Aggregation Using Reconfigurable Hardware  
(Prajith Ramakrishnan Gethakumari, Vincenzo Gulisano, Bo Joel Svensson, Pedro Trancoso, Ioannis Sourdis)
## 5. Crypto & Networking

<table>
<thead>
<tr>
<th>Page</th>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>120</td>
<td>Toward a New HLS-Based Methodology for FPGA Benchmarking of Candidates in Cryptographic Competitions: The CAESAR Contest Case Study</td>
<td>Ekawat Homsirikamol, Kris Gaj</td>
</tr>
<tr>
<td>128</td>
<td>Comparing the Cost of Protecting Selected Lightweight Block Ciphers Against Differential Power Analysis in Low-Cost FPGAs</td>
<td>William Diehl, Abubakr Abdulgadir, Jens-Peter Kaps, Kris Gaj</td>
</tr>
<tr>
<td>136</td>
<td>Accelerating NFV Application Using CPU-FPGA Tightly Coupled Architecture</td>
<td>Yoshikazu Watanabe, Yuki Kobayashi, Takashi Takenaka, Takeo Hosomi, Yuichi Nakamura</td>
</tr>
</tbody>
</table>

## 6. ML/Vision I

<table>
<thead>
<tr>
<th>Page</th>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>144</td>
<td>An Energy Efficient Approach for C4.5 Algorithm Using OpenCL Design Flow</td>
<td>Hai Peng, Xiaofan Zhang, Letian Huang</td>
</tr>
<tr>
<td>152</td>
<td>Exploring Automated Space/Time Tradeoffs for OpenVX Compute Graphs</td>
<td>Hossein Omidian, Guy G.F. Lemieux</td>
</tr>
<tr>
<td>160</td>
<td>NnCore: A Parameterized Non-Linear Function Generator for Machine Learning Applications in FPGAs</td>
<td>Sam M.H. Ho, Hayden Kwok-Hay So</td>
</tr>
</tbody>
</table>

## 7. ML/Vision II

<table>
<thead>
<tr>
<th>Page</th>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>168</td>
<td>An Object Detector Based on Multiscale Sliding Window Search Using a Fully Pipelined Binarized CNN on an FPGA</td>
<td>Hiroki Nakahara, Haruyoshi Yonekawa, Shimpei Sato</td>
</tr>
<tr>
<td>176</td>
<td>Lowering Dynamic Power in Stream-Based Harris Corner Detection Architecture</td>
<td>Siew-Kei Lam, Rakesh Kumar Bijarniya, Meiqing Wu</td>
</tr>
<tr>
<td>183</td>
<td>A 42fps Full-HD ORB Feature Extraction Accelerator with Reduced Memory Overhead</td>
<td>Rongdi Sun, Pelin Liu, Jun Wang, Cecil Accetti, Abid A. Naqvi</td>
</tr>
</tbody>
</table>
ICFPT 2017 Table of Contents

Poster Papers

191 A Scalable Hybrid Architecture for High Performance Data-Parallel Applications
(Moucheng Yang, Jifang Jin, Zhehao Li, Xuegong Zhou, Shaojun Wang, Lingli Wang)

195 Homeostatic Fault Tolerance in Spiking Neural Networks Utilizing Dynamic Partial
Reconfiguration of FPGAs
(Anju P. Johnson, Junxia Liu, Alan G. Millard, Shvan Karim, Andy M. Tyrrell, Jim Harkin,
Jon Timmis, Liam McDaid, David M. Halliday)

199 Model-Based Hardware Design Based on Compatible Sets of Isomorphic Subgraphs
(Patrick Sittel, Konrad Möller, Martin Kumm, Peter Zipf, Bogdan Pasca, Mark Jervis)

203 A NoC-Based Custom FPGA Configuration Memory Architecture for Ultra-Fast
Micro-Reconfiguration
(Amit Kulkarni, Poona Bahrebar, Dirk Stroobandt, Giulio Stramondo,
Cătălin Bogdan Ciobanu, Ana Lucia Varbanescu)

207 An FPGA-Based Processor for Training Convolutional Neural Networks
(Zhiqiang Liu, Yong Dou, Jingfei Jiang, Qiang Wang, Paul Chow)

211 An FPGA-Accelerated High-Throughput Data Optimization System for High-Speed
Transfer via Wide Area Network
(Kentaro Katayama, Hidetoshi Matsumura, Hiroaki Kameyama, Shinichi Sazawa,
Yasuhiro Watanabe)

215 Evolvable Caches: Optimization of Reconfigurable Cache Mappings for a
LEON3/Linux-Based Multi-Core Processor
(Nam Ho, Paul Kaufmann, Marco Platzner)

219 An Open Source PXIe Ecosystem Based on FPGA Modules
(Andrew Ang, Matt Bourne, Robin Dykstra)

223 FPGA-Based High-Performance Time-to-Digital Converters by Utilizing Multi-Channels
Looped Carry Chains
(Ke Cui, Zongkai Liu, Rihong Zhu, Xiangyu Li)

227 Instruction Driven Cross-Layer CNN Accelerator with Winograd Transformation on
FPGA
(Jincheng Yu, Yiming Hu, Xuefeng Ning, Jiantao Qiu, Kaiyuan Guo, Yu Wang, Huazhong Yang)

231 An FPGA-Based Tree Crown Detection Approach for Remote Sensing Images
(Wei Li, Conghui He, Haoqian Hu, Wayne Luk)

235 A Light-Weight Hardware/Software Co-Design for Pairing-Based Cryptography with Low
Power and Energy Consumption
(Ahmad Salman, William Diehl, Jens-Peter Kaps)

239 FPGA-Based Training of Convolutional Neural Networks with a Reduced Precision
Floating-Point Library
(Roberto DiCecco, Lin Sun, Paul Chow)

243 Selection of an Error-Correcting Code for FPGA-Based Physical Unclonable Functions
(Brian Jarvis, Kris Gaj)

247 Streaming Sorting Network Based BWT Acceleration on FPGA for Lossless Compression
(Baoju Zhao, Yubin Li, Yu Wang, Huazhong Yang)

251 Runtime Rule-Reconfigurable High Throughput NIPS on FPGA
(P.M.K. Tharaka, D.M.D. Wijerathne, Navoda Perera, Dinushan Vishwajith, Ajith Pasqual)

255 Designing and Accelerating Spiking Neural Networks Using OpenCL for FPGAs
(Artur Podobas, Satoshi Matsuoka)

Poster Papers continues next page...
ICFPT 2017 Table of Contents

**Poster Papers continued…**

<table>
<thead>
<tr>
<th>Page</th>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>259</td>
<td><strong>Customizable FPGA OpenCL Matrix Multiply Design Template for Deep Neural Networks</strong></td>
<td>Jack Yinger, Eriko Nurvitadhi, Davor Capalija, Andrew Ling, Debbie Marr, Srivatsan Krishnan, Duncan Moss, Suchit Subhaschandra</td>
</tr>
<tr>
<td>263</td>
<td><strong>A Comprehensive Hardware/Software Infrastructure for IP Cores Design Protection</strong></td>
<td>Brice Colombier, Lilian Bossuet, Ugo Mureddu, David Hély</td>
</tr>
<tr>
<td>267</td>
<td><strong>hCODE 2.0: An Open-Source Toolkit for Building Efficient FPGA-Enabled Clouds</strong></td>
<td>Qian Zhao, Hendarmawan, Motoki Amagasaki, Masahiro Iida, Norhiro Kuga, Toshinori Sueyoshi</td>
</tr>
<tr>
<td>271</td>
<td><strong>Calling Hardware Procedures in a Reconfigurable accelerator Using RPC-FPGA</strong></td>
<td>Erik H. D’Hollander, Bruno Chevalier, Koen De Bosschere</td>
</tr>
<tr>
<td>275</td>
<td><strong>FPGA-Based ORB Feature Extraction for Real-Time Visual SLAM</strong></td>
<td>Weikang Fang, Yanjun Zhang, Bo Yu, Shaoshan Liu</td>
</tr>
</tbody>
</table>

**Demo Session**

<table>
<thead>
<tr>
<th>Page</th>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>279</td>
<td><strong>PipeCNN: An OpenCL-Based Open-Source FPGA Accelerator for Convolution Neural Networks</strong></td>
<td>Dong Wang, Ke Xu, Diankun Jiang</td>
</tr>
<tr>
<td>283</td>
<td><strong>Hough Transform Line Reconstruction on FPGA Using Back-Projection</strong></td>
<td>Donald G. Bailey</td>
</tr>
<tr>
<td>287</td>
<td><strong>FPGA Implementation of Convolutional Neural Network Based on Stochastic Computing</strong></td>
<td>Daewoo Kim, Mansureh S. Moghaddam, Hossein Moradian, Hyeonuk Sim, Jongeun Lee, Kiyoung Choi</td>
</tr>
</tbody>
</table>

**Design Competition**

<table>
<thead>
<tr>
<th>Page</th>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>291</td>
<td><strong>All Binarized Convolutional Neural Network and its Implementation on an FPGA</strong></td>
<td>Masayuki Shimoda, Shimpei Sato, Hiroki Nakahara</td>
</tr>
<tr>
<td>295</td>
<td><strong>FPGA-Based Accelerator for Losslessly Quantized Convolutional Neural Networks</strong></td>
<td>Mankit Sit, Ryosuke Kazami, Hideharu Amano</td>
</tr>
</tbody>
</table>

**PhD Forum**

<table>
<thead>
<tr>
<th>Page</th>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>299</td>
<td><strong>FPGA Implementation of a Real-Time Super-Resolution System with a CNN Based on a Residue Number System</strong></td>
<td>Taito Manabe, Yuichiro Shibata, Kiyoshi Oguri</td>
</tr>
<tr>
<td>301</td>
<td><strong>A Unified Reconfigurable Floating-Point Arithmetic Architecture Based on CORDIC Algorithm</strong></td>
<td>Bingyi Li, Linlin Fang, Yizhuang Xie, He Chen, Liang Chen</td>
</tr>
</tbody>
</table>