2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC 2018)

Jeju, South Korea
22 – 25 January 2018
**1K Opening & Keynote I**

Time: 9:00 - 10:30, Tuesday, January 23, 2018
Location: Halla Hall
Chair: Youngsoo Shin (KAIST, Republic of Korea)

1K-1 (Time: 9:30 - 10:30)
(Keynote Address) Designing Heterogeneous Systems in the AI Era: Challenges and Opportunities
Jeff Burns (IBM, U.S.A.)

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**1A (SS-1) Deep Learning for Applications that Live on Big Data**

Time: 11:00 - 12:15, Tuesday, January 23, 2018
Location: Room 302
Organizer: Deming Chen (Univ. of Illinois, Urbana-Champaign)

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Location: Room 401
Chairs: Ji-Hoon Kim (Seoul National Univ. of Science and Tech., Republic of Korea), Youngjoo Lee (POSTECH, Republic of Korea)

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Time: 11:00 - 12:15, Tuesday, January 23, 2018
Location: Room 402A
Chairs: Yanzhi Wang (Syracuse Univ., U.S.A.), Juinn-Dar Huang (National Chiao Tung Univ., Taiwan)

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Location: Room 302
Organizer: Gang Qu (Univ. of Maryland, U.S.A.)

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Location: Halla Hall
Chair: Youngsoo Shin (KAIST, Republic of Korea)

2K-1  (Time: 9:00 - 10:00)
(Keynote Address) Quality, Schedule and Cost: Design Technology and the Last Semiconductor Scaling Levers
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Time:  10:30 - 12:10, Wednesday, January 24, 2018
Location: Room 302
Chairs: Minkyu Je (KAIST, Republic of Korea), Ikjoon Chang (Kyung Hee Univ., Republic of Korea)

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4B  System Architectures
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Chairs: Sri Parameswaran (Univ. of New South Wales, Australia), Jing-Jia Liou (National Tsing Hua Univ., Taiwan)

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<td>*Hongbin Zhang (Tsinghua Univ., China), Chao Zhang (Peking Univ., China), Qingda Hu (Tsinghua Univ., China), Chengmo Yang (Univ. of Delaware, U.S.A.), Jiwu Shu (Tsinghua Univ., China)</td>
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<td>Modeling of Biaxial Magnetic Tunneling Junction for Multi-level Cell STT-RAM Realization</td>
<td>Enes Eken, Ismail Bayram (Univ. of Pittsburgh, U.S.A.), Hai (Helen) Li, *Yiran Chen (Duke Univ., U.S.A.)</td>
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<td>Automatic Insertion of Airgap with Design Rule Constraints</td>
<td>*Daijoon Hyun, Youngsoo Shin (KAIST, Republic of Korea)</td>
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<td>Dai Feng Guo (Univ. of Illinois, Urbana-Champaign, U.S.A.), Hongbo Zhang (Facebook, U.S.A.), *Martin D.F. Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.)</td>
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<td>Lifetime-aware Design Methodology for Dynamic Partially Reconfigurable Systems</td>
<td>*Siva Satyendra Sahoo, Tuan D. A. Nguyen, Bharadwaj Veeravalli (National Univ. of Singapore, Singapore), Akash Kumar (Tech. Univ. Dresden, Germany)</td>
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<td><strong>4D-4</strong></td>
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<td>Electromigration-Lifetime Constrained Power Grid Optimization Considering Multi-Segment Interconnect Wires</td>
<td>Han Zhou, Yijing Sun, Zeyu Sun, Hengyang Zhao, *Sheldon X.-D. Tan (Univ. of California, Riverside, U.S.A.)</td>
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<td><strong>Machine/Deep Learning for Semiconductor Design, EDA Technologies, and Application</strong></td>
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<td>*Andrew B. Kahng (Univ. of California, San Diego, U.S.A.)</td>
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<td>*Manish Pandey (Synopsys, U.S.A.)</td>
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<td>(Time: 15:20 - 15:45)</td>
<td>Large-scale Short-term Urban Taxi Demand Forecasting Using Deep Learning</td>
<td>Siyu Liao (City Univ. of New York, U.S.A.), Liutong Zhou, Xuan Di (Columbia Univ., U.S.A.), Bo Yuan (City Univ. of New York, U.S.A.), *Jinjun Xiong (IBM, U.S.A.)</td>
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### 5B  System Design Methodologies

**Time:** 13:40 - 15:45, Wednesday, January 24, 2018  
**Location:** Room 401  
**Chairs:** Naehyuck Chang (KAIST, Republic of Korea), Akash Kumar (Tech. Univ. Dresden, Germany)

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<td>Utilizing Quad-Trees for Efficient Design Space Exploration with Partial Assignment Evaluation</td>
<td>*Kai Neubauer (Univ. of Rostock, Germany), Philipp Wanko, Torsten Schaub (Univ. of Potsdam, Germany), Christian Haubelt (Univ. of Rostock, Germany)</td>
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<td>SCBench: A Benchmark Design Suite for SystemC Verification and Validation</td>
<td>*Bin Lin, Fei Xie (Portland State Univ., U.S.A.)</td>
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<td>5B-3</td>
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<td>MemFlow: Memory-Driven Data Scheduling with Datapath Co-design in Accelerators for Large-Scale Inference Applications</td>
<td>*Qi Nie, Sharad Malik (Princeton Univ., U.S.A.)</td>
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<td>A Mapping Approach between IR and Binary CFGs Dealing with Aggressive Compiler Optimizations for Performance Estimation</td>
<td>*Omayma Matoussi, Frédéric Pétrot (Tima Laboratory, Grenoble INP, France)</td>
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<td>15:20 - 15:45</td>
<td>System Level Performance Analysis and Optimization for the Adaptive Clocking based Multi-Core Processor</td>
<td>*Byung Su Kim (Samsung Electronics, Republic of Korea), Joon-Sung Yang (Sungkyunkwan Univ., Republic of Korea)</td>
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### 5C  Synthesis, Routing and Timing

**Time:** 13:40 - 15:45, Wednesday, January 24, 2018  
**Location:** Room 402A  
**Chairs:** Jason C. Verley (Sandia National Laboratory, U.S.A.), Mark Po-Hung Lin (National Chung Cheng Univ., Taiwan)

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<td>Detecting Non-Functional Circuit Activity in SoC Designs</td>
<td>*Dustin Peterson, Yannick Boeckle, Oliver Bringmann (Univ. of Tübingen, Germany)</td>
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<td>5C-2</td>
<td>14:05 - 14:30</td>
<td>Multi-Level Timing Simulation on GPUs</td>
<td>*Eric Schneider, Michael A. Kochte, Hans-Joachim Wunderlich (Univ. of Stuttgart, Germany)</td>
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<td>An Optimal Gate Design for the Synthesis of Ternary Logic Circuits</td>
<td>*Sunmean Kim, Taeho Lim, Seokhyeong Kang (Ulsan National Inst. of Science and Tech., Republic of Korea)</td>
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<td>Performance-Preserved Analog Routing Methodology via Wire Load Reduction</td>
<td>*Hao-Yu Chi, Hwa-Yi Tseng, Chien-Nan Jimmy Liu (National Central Univ., Taiwan), Hung-Ming Chen (National Chiao Tung Univ., Taiwan)</td>
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<td>Static Timing Analysis for Ring Oscillators</td>
<td>*David M. Moore (Univ. of Michigan, U.S.A.), Jeffrey A. Fredenburg, Muhammad Faisal ( Movellus, U.S.A.), David D. Wentzlaff (Univ. of Michigan, U.S.A.)</td>
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Time: 13:40 - 15:45, Wednesday, January 24, 2018
Location: Room 402B
Chairs: Yasuhiro Takashima (Univ. of Kitakyushu, Japan), Ting-Chi Wang (National Tsing Hua Univ., Taiwan)

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Time: 16:15 - 17:30, Wednesday, January 24, 2018
Location: Room 302
Organizer: Kiyoung Choi (Seoul National Univ., Republic of Korea)

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6B  Emerging Memory Management Techniques

Time: 16:15 - 17:30, Wednesday, January 24, 2018
Location: Room 401
Chairs: Minsoo Rhu (POSTECH, Republic of Korea), Pi-Cheng Hsiu (Academia Sinica, Taiwan)

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<td>*Matthias Becker, Saad Mubeen (Mälardalen Univ., Sweden), Dakshina Dasari (Robert Bosch GmbH, Germany), Moris Behnam, Thomas Nolte (Mälardalen Univ., Sweden)</td>
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<td>Fully Parallel RRAM Synaptic Array for Implementing Binary Neural Network with (+1, -1) Weights and (+1, 0) Neurons</td>
<td>Xiaoyu Sun, Xiaochen Peng, Pai-Yu Chen, Rui Liu, Jae-sun Seo, *Shimeng Yu (Arizona State Univ., U.S.A.)</td>
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<td>*Bruno Schmitt (EPFL, Switzerland), Alan Mishchenko, Robert Brayton (UC Berkeley, U.S.A.)</td>
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<td>A Two-Step Search Engine for Large Scale Boolean Matching under NP3 Equivalence</td>
<td>*Chak-Wa Pui, Peishan Tu, Haocheng Li, Gengjie Chen, Evangeline F.Y. Young (Chinese Univ. of Hong Kong, Hong Kong)</td>
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<td>Low-Cost Hardware Architectures for Mersenne Modulo Functional Units</td>
<td>Keith Campbell, Chen-Hsuan Lin, *Deming Chen (Univ. of Illinois, Urbana-Champaign, U.S.A.)</td>
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3K  Keynote III
Time: 8:30 - 10:00, Thursday, January 25, 2018
Location: Halla Hall
Chair: Youngsoo Shin (KAIST, Republic of Korea)

3K-1 (Time: 8:30 - 9:15)
(Keynote Address) CAE Challenge on High Capacity/High Bandwidth Memory Design
Woojong Han (SK Hynix, Republic of Korea)

3K-2 (Time: 9:15 - 10:00)
(Keynote Address) Terabyte/s Bandwidth 2.5D HBM (High-bandwidth Memory Module) Designs for Deep Learning Artificial Intelligent Servers
Joungho Kim (KAIST, Republic of Korea)

7A  Multiplier Design: From Accurate to Approximate
Time: 10:30 - 11:45, Thursday, January 25, 2018
Location: Room 302
Chairs: Kazuyoshi Takagi (Kyoto Univ., Japan), Youngjoo Lee (POSTECH)

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*Min Soo Kim (Univ. of California, Irvine, U.S.A.), Alberto Antonio Del Barrio, Román Hermida (Univ. Complutense de Madrid, Spain), Nader Bagherzadeh (Univ. of California, Irvine, U.S.A.)

7B  (SS-4) Reliability and Aging-Aware Designs for sub-10nm ICs
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Location: Room 401
Organizer: Sheldon Tan (UC Riverside, U.S.A.)

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7B-3 (Time: 11:20 - 11:45)
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<td>Mehdi Tahoori (Karlsruhe Inst. of Tech., Germany), Jim Huang (Hewlett Packard Labs)</td>
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7C-1 (Time: 10:30 - 10:55)  
(Invited Paper) Mechanical Strain and Temperature Aware Design Methodology for Thin-Film Transistor Based Pseudo-CMOS Logic Array  
*Wenyu Sun, Yuxuan Huang, Qinghang Zhao, Fei Qiao (Tsinghua Univ., China), Tsung-Yi Ho (National Tsing Hua Univ., Taiwan), Xiaojun Guo (Shanghai Jiao Tong Univ., China), Huazhong Yang, Yongpan Liu (Tsinghua Univ., China)  

7C-2 (Time: 10:55 - 11:20)  
(Invited Paper) Process Design Kit for Flexible Hybrid Electronics  
*Leilai Shao (UCSB, U.S.A.), Tsung-Ching Huang (Hewlett Packard Labs, U.S.A.), Ting Lei, Zhenan Bao (Stanford Univ., U.S.A.), Raymond Beausoleil (Hewlett Packard Labs, U.S.A.), Kwang-Ting Cheng (Hong-Kong Univ. of Science and Tech., China)  

7C-3 (Time: 11:20 - 11:45)  
(Invited Paper) From Silicon to Printed Electronics: A Coherent Modeling and Design Flow Approach Based on Printed Electrolyte Gated FETs  
Gabriel Cadilha Marques, Farhan Rasheed, Jasmin Aghassi-Hagmann, *Mehdi B. Tahoori (Karlsruhe Inst. of Tech., Germany)  

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<td>Kyu-Myung Choi (Seoul National Univ., Republic of Korea), Sangdo Park (Samsung Electronics, Republic of Korea)</td>
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7D-1 (Time: 10:30 - 10:55)  
A Best-Fit Mapping Algorithm to Facilitate ESOP-Decomposition in Clifford+T Quantum Network Synthesis  
*Giulia Meuli, Mathias Soeken (EPFL, Switzerland), Martin Roetteler, Nathan Wiebe (Microsoft Research, U.S.A.), Giovanni De Micheli (EPFL, Switzerland)  

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*Alwin Zulehner, Robert Wille (Johannes Kepler Univ. Linz, Austria)  

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*Zhufei Chu (Ningbo Univ., China), Mathias Soeken (EPFL, Switzerland), Yinshui Xia (Ningbo Univ., China), Giovanni De Micheli (EPFL, Switzerland)  

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CANNA: Neural Network Acceleration using Configurable Approximation on GPGPU  
Mohsen Imani, Max Masich, *Daniel Peroni, Pushen Wang, Tajana Rosing (Univ. of California, San Diego, U.S.A.)  

8A-2 (Time: 13:40 - 14:05)  
Task Assignment and Scheduling in MPSoC under Process Variation: A Stochastic Approach  
*Behnam Khodabandeloo, Ahmad Khonsari (Univ. of Tehran/Institute for Research in Fundamental Sciences, Iran), Alireza Majidi (Texas A&M Univ., U.S.A.), Mohammad Hassan Hajiesmaili (Univ. of Tehran/Institute for Research in Fundamental Sciences, Iran)
9A Hardware Security Primitive Design and Implementation

Time: 15:00 - 16:15, Thursday, January 25, 2018
Location: Room 302
Chairs: Wujie Wen (Florida International Univ., U.S.A.), Taewhan Kim (Seoul National Univ., Republic of Korea)

9A-1 (Time: 15:00 - 15:25)
CryptoBlaze: A Partially Homomorphic Processor with Multiple Instructions and Non-Deterministic Encryption Support
*Florencia Irena, Daniel Murphy, Sri Parameswaran (Univ. of New South Wales, Australia)

9A-2 (Time: 15:25 - 15:50)
PMU-Trojan: On Exploiting Power Management Side Channel for Information Leakage
*Md Nazmul Islam, Sandip Kundu (Univ. of Massachusetts Amherst, U.S.A.)

9A-3 (Time: 15:50 - 16:15)
A Low-overhead PUF based on Parallel Scan Design
*Wenxuan Wang, Aijiao Cui (Harbin Inst. of Tech. Shenzhen Graduate School, China), Gang Qu (Univ. of Maryland, U.S.A.), Huawei Li (Chinese Academy of Sciences, China)

10A Deep Learning and Architectural Security

Time: 16:45 - 18:00, Thursday, January 25, 2018
Location: Room 302
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Atul Prasad Deb Nath (Univ. of Florida, U.S.A.), Sandip Ray (NXP Semiconductors, U.S.A.), Abhishek Basak (Intel, U.S.A.), Swarup Bhunia (Univ. of Florida, U.S.A.)